Root Cause Analysis for Via Hole Faults Using Digital Twin

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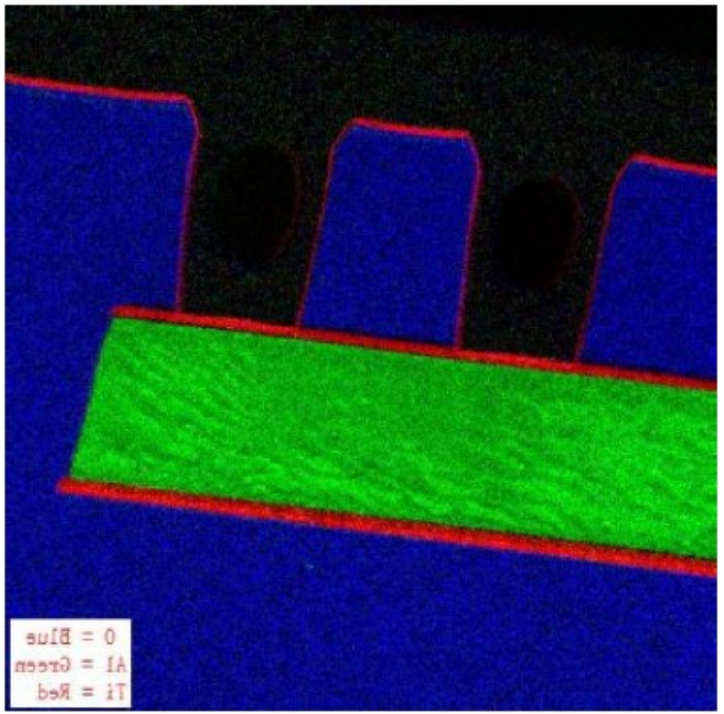
Content

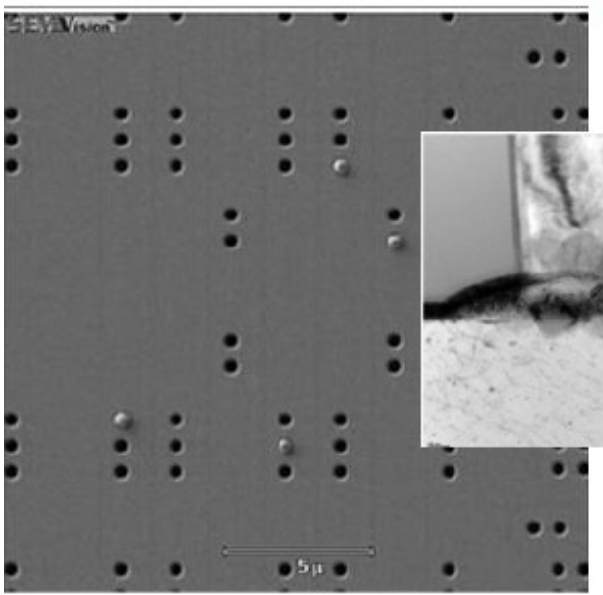
- Problem description
- Digital twin – the methodology
- Equipment model
- Process models
  - Electrical 3d wafer heating model
  - Thermal wafer model
- Temperature distribution with parameter variation
- Solution of process problem
- Conclusions

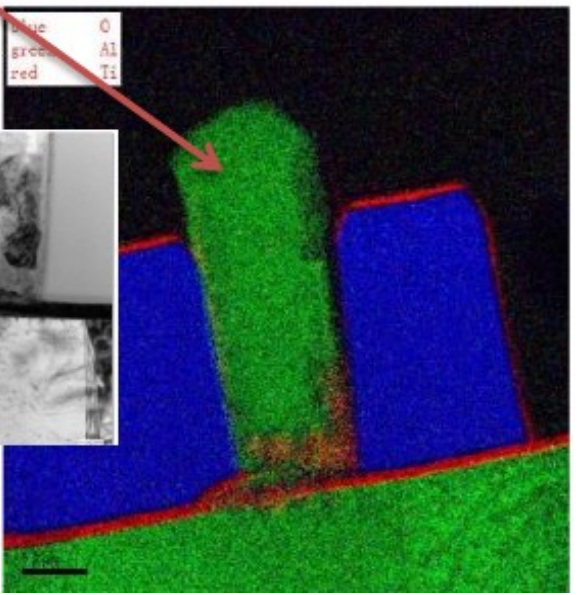
The Problem: Via Al Up Extrusions

Good site



Bad site with Al up extrusion





First Steps in Every Process Problem

- Problem description of wafer and device level

  Usually good data

- Is the problem visible in tool / FDC data?
  Very often the answer is unfortunately no !

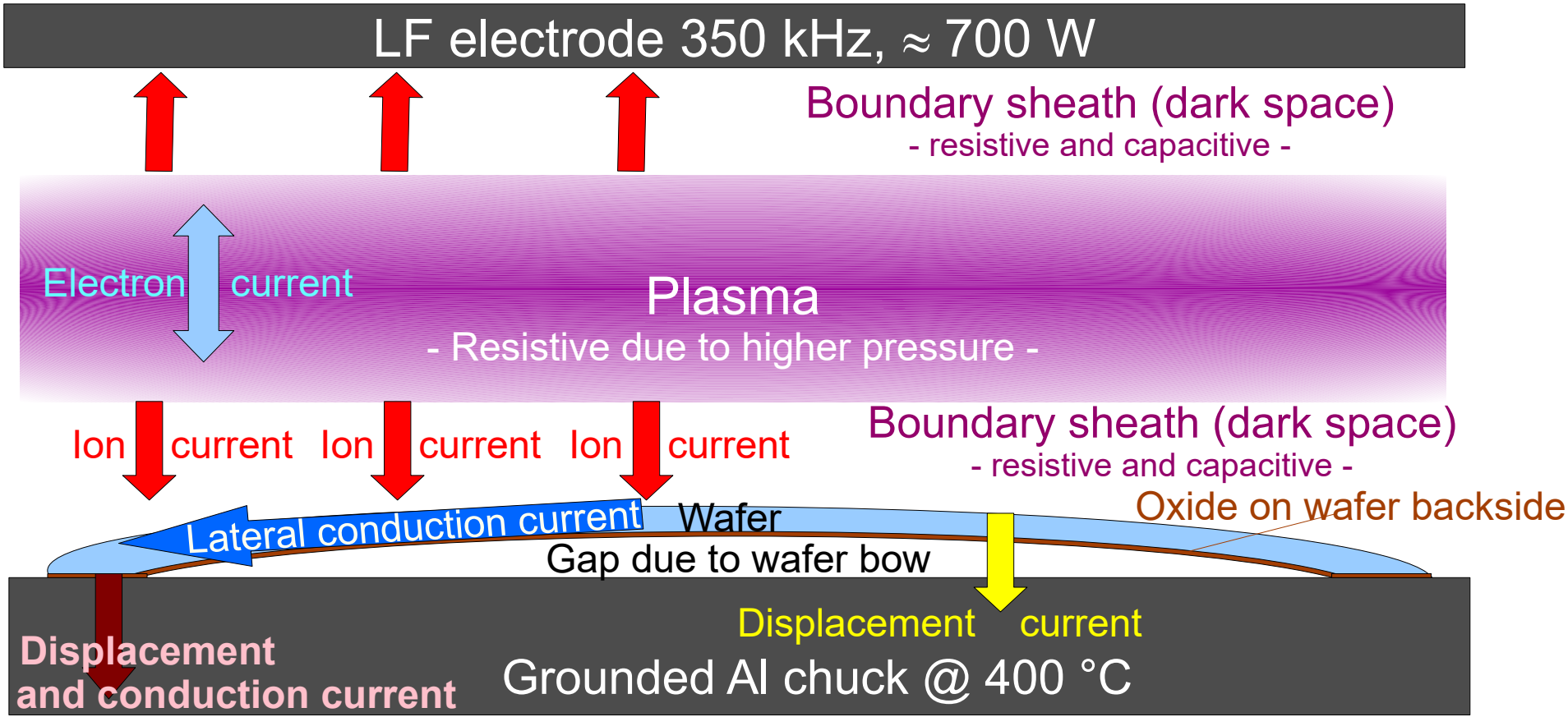
  No data quality analysis of tools data.
  Bad tool data quality.

- How to get reasonable data ?

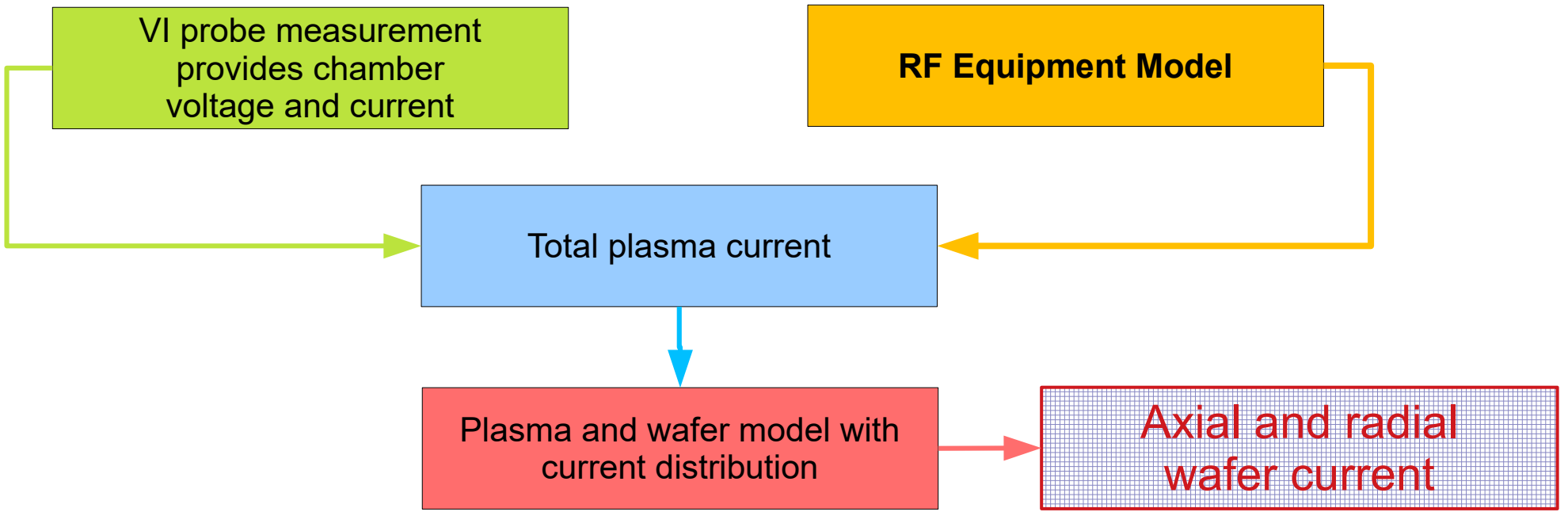
  Off-line measurements for equipment model
  On-line measurement for process model, also based on equipment model

  → **Main parts of a digital twin**

Scheme of 200 mm Chamber and Process

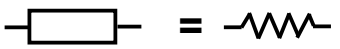


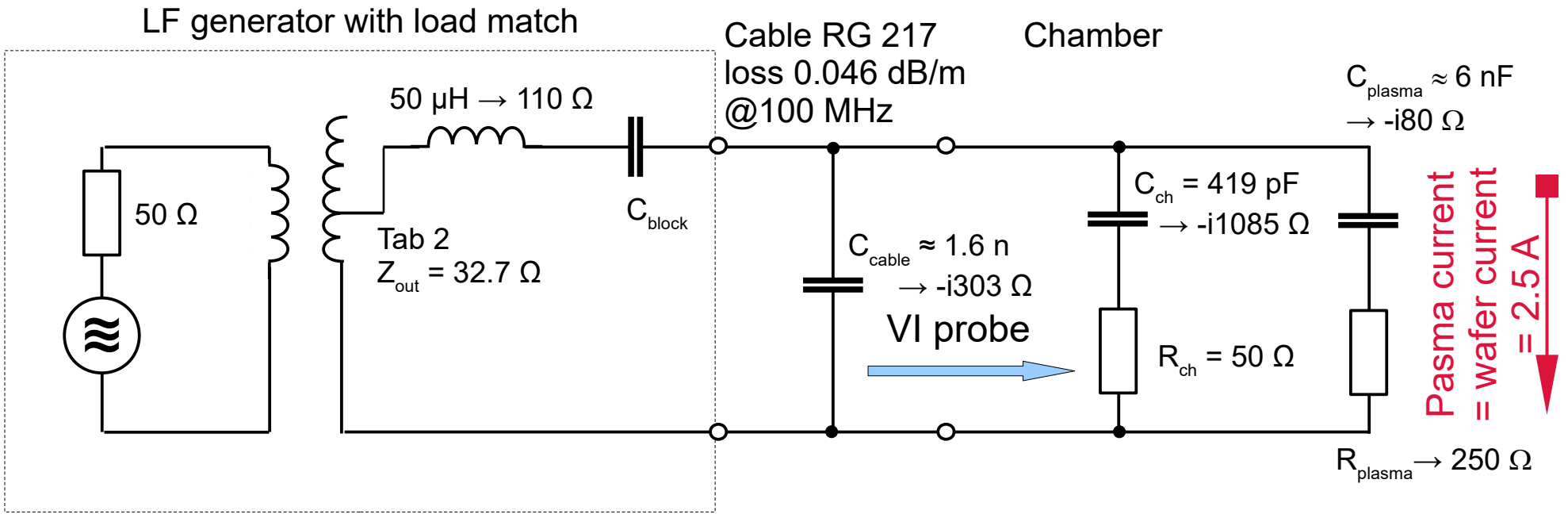
The Digital Twin – I. Wafer Current



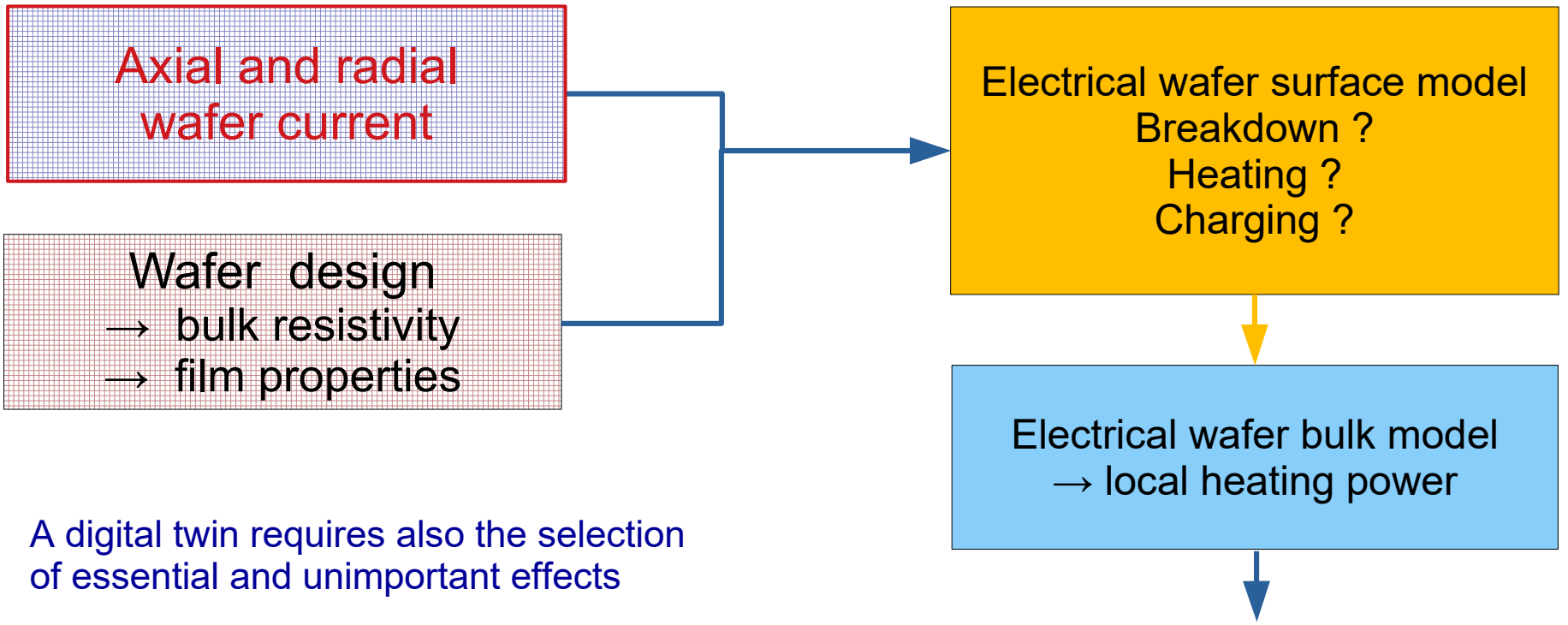
Equivalent circuit of generator, chamber, and plasma

- Parametrization by
  - off-line measurement → RF equipment model (chamber w/o plasma)
  - In-line measurement → VI probe (process)
- Plasma is dominant resistive.





The Digital Twin – Part II



- A digital twin requires also the selection of essential and unimportant effects

Electrical equations and boundary conditions

- Given:

$$|\vec{j}_{LF,plasma}| \;\; with \;\; \frac{d\,\vec{j}_{LF}}{d\,r} = 0 \;\wedge\; |Z_{wafer,chuck}| \;\; with \;\; \frac{d\,Z_{wafer,chuck}}{d\,r} = 0$$

from total current measured by VI probe with correction from RF equipment model for chamber impedance.
Equations, all variables are complex and so comprising displacement and conduction current:

$$\nabla \vec{j}_{tot} = \nabla \left(\vec{j}_{conduction} + \vec{j}_{displacement}\right) = 0$$

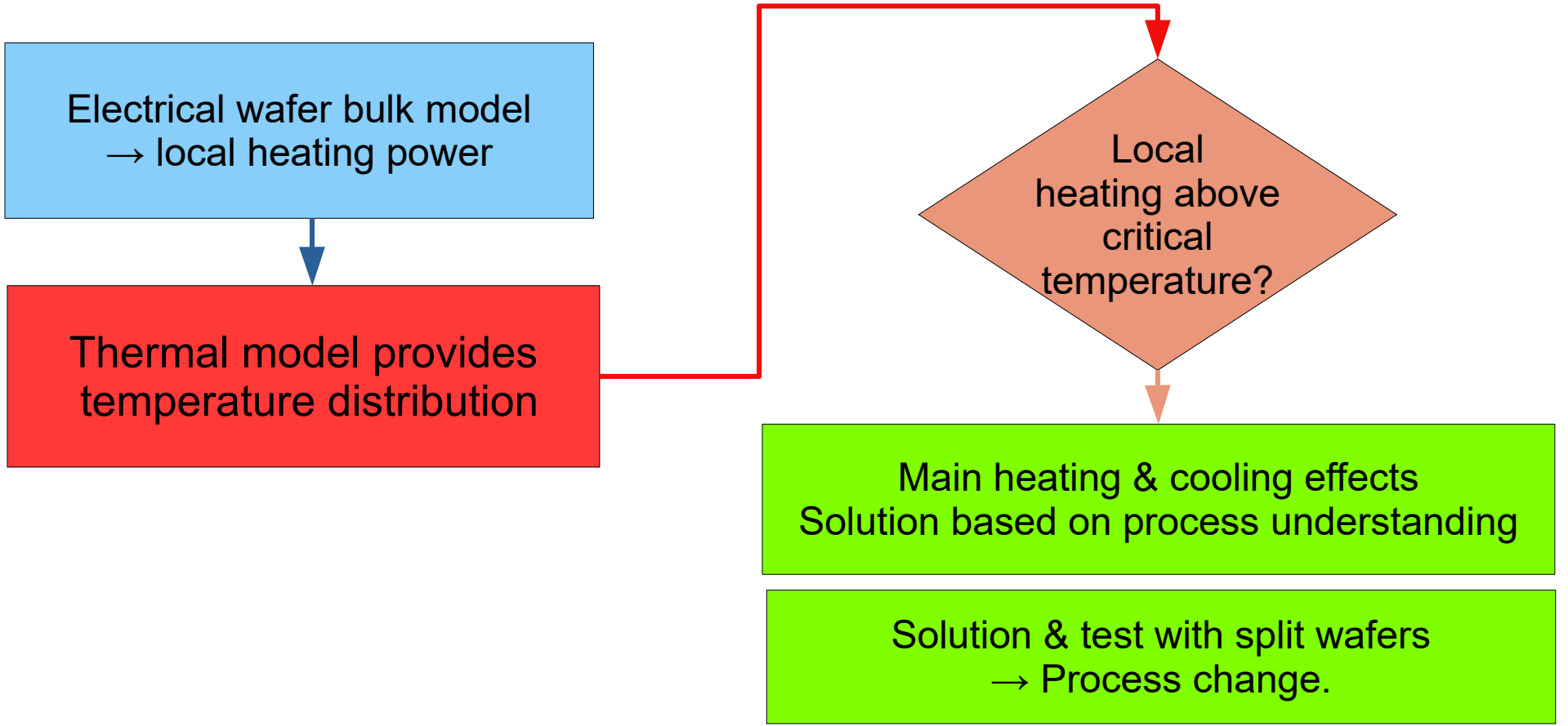
- Conductivity and thickness of wafer (bulk) and wafer backside (SiO_2), wafer bow, wafer temperature, melting temperature of aluminum at process pressure.

Output

$$\vec{j}_{tot,wafer}(r,\varphi) = \mathrm{i}\,\omega\,\underline{\epsilon}\,\vec{E}(r,\varphi)$$

$$P_{wafer,V}(r,\varphi) = \Re\left[\vec{E}(r,\varphi)\cdot\vec{j}^{\,*}_{tot}\right]$$

The Digital Twin – Part III



Heat equations and boundary conditions

- The thermal model includes
  - Electrical heating from electrical model
  - Heat conduction at contact
  - Heat capacitance (const. but T spatially resolved)
  - Radiation → very important

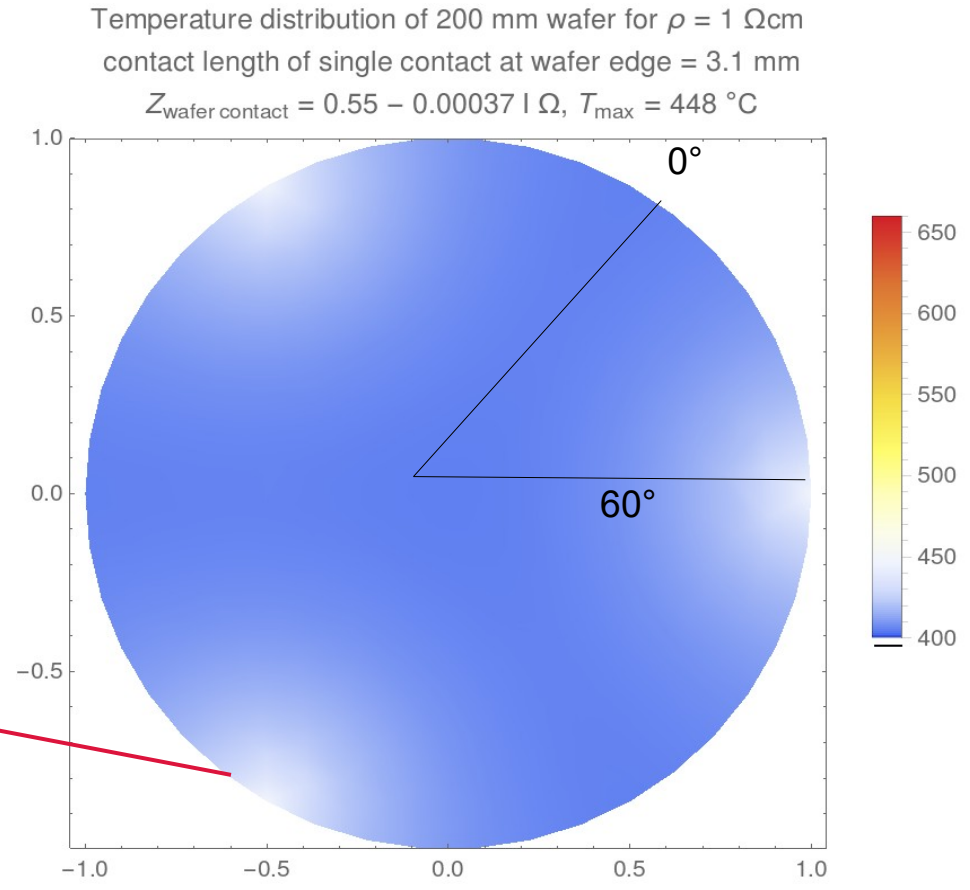
- This lead finally to the PDE for the temperature:

$$\rho\, c_{Si}\, \dot{T}(t,r,\varphi) = \lambda\, \nabla^2 T(t,r,\varphi) + P_{wafer,V}(t,r,\varphi) + \epsilon\sigma\, T^4(t,r,\varphi)/d_{wafer}$$

Output

$$T(t,r,\varphi)$$

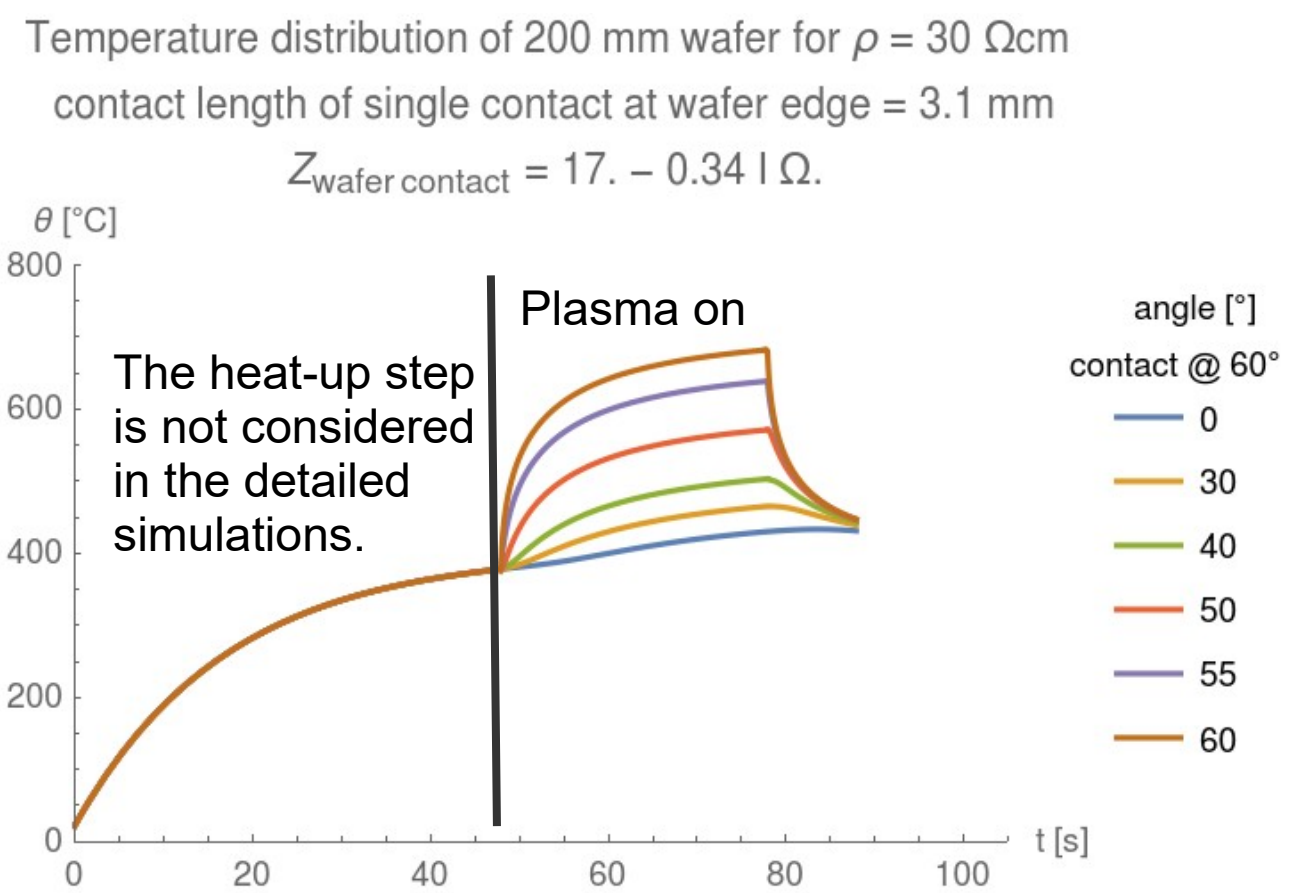
Typical Temperature Map at Process End



Contact point with high current density

Process overview – heat-up and plasma steps

- Cold wafer is put on chuck with 400°C.
- Despite three single contact point of the wafer, radiation provides a very homogeneous temperature distribution.
- The plasma step shows the impact of the single points.
- After heat-up the temperature is close to 400°C, can be assumed as initial condition of the plasma step.



Model Variations

- Wafer resistivity

  Dependence on product / technology

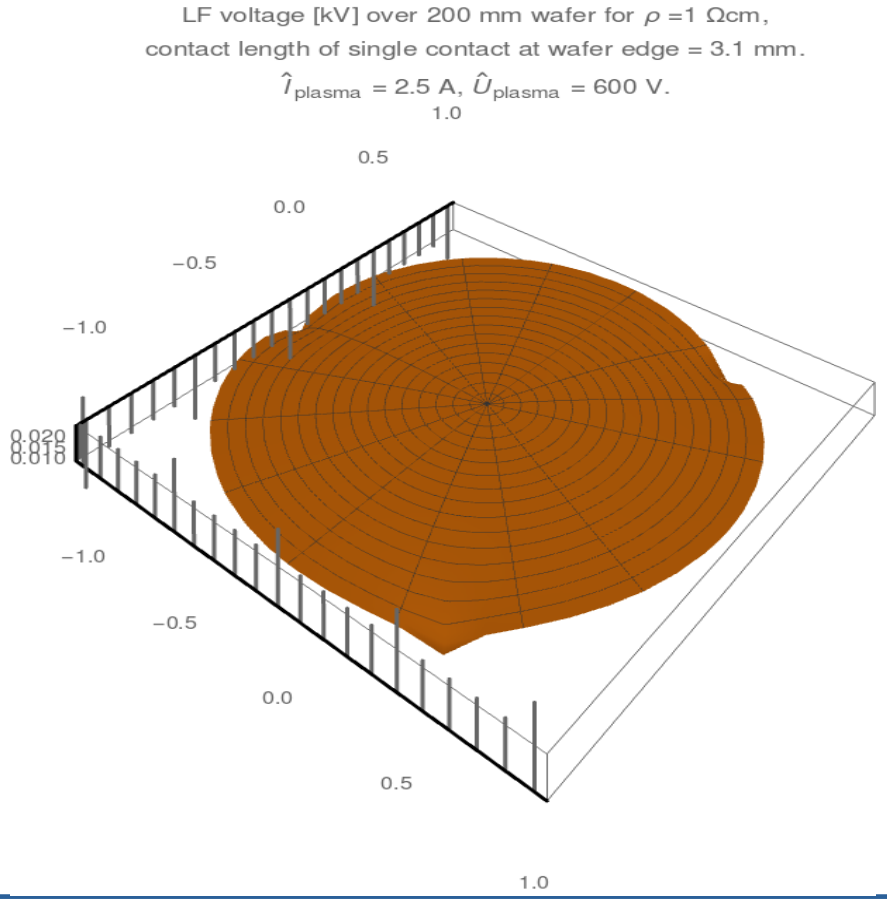
- Contact area to chuck

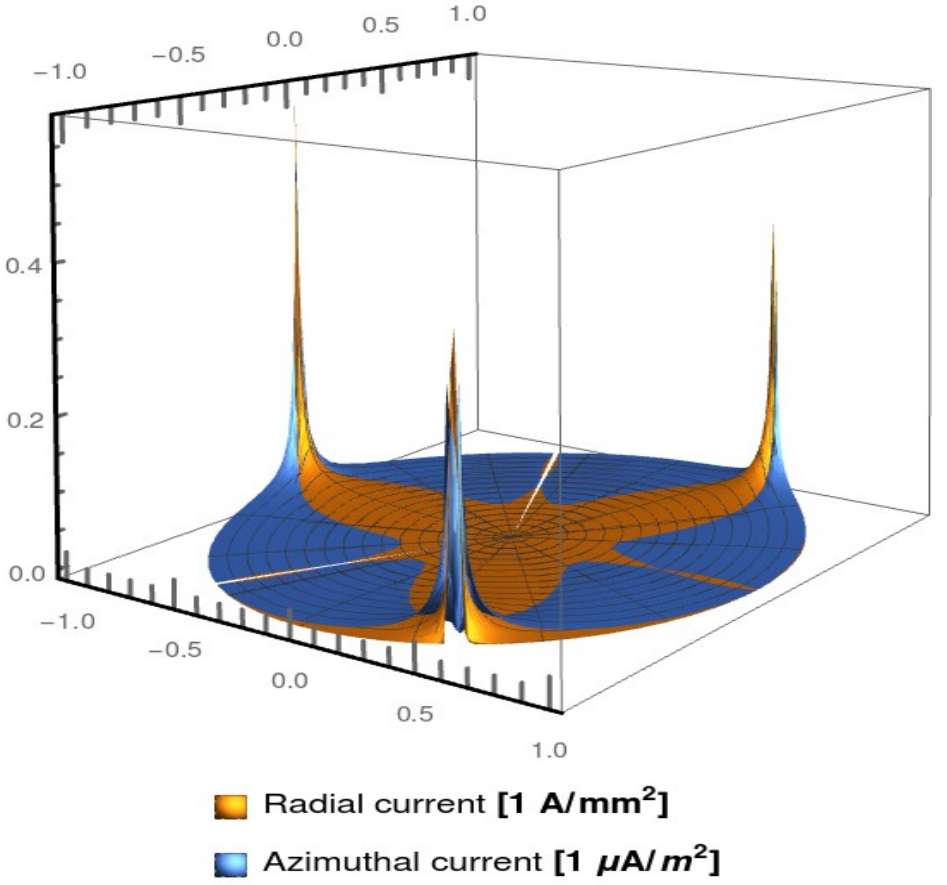
  Show potential influence of
  - wafer handling
  - chuck refurbishment
  - wafer BS

- Chuck temperature & LF power

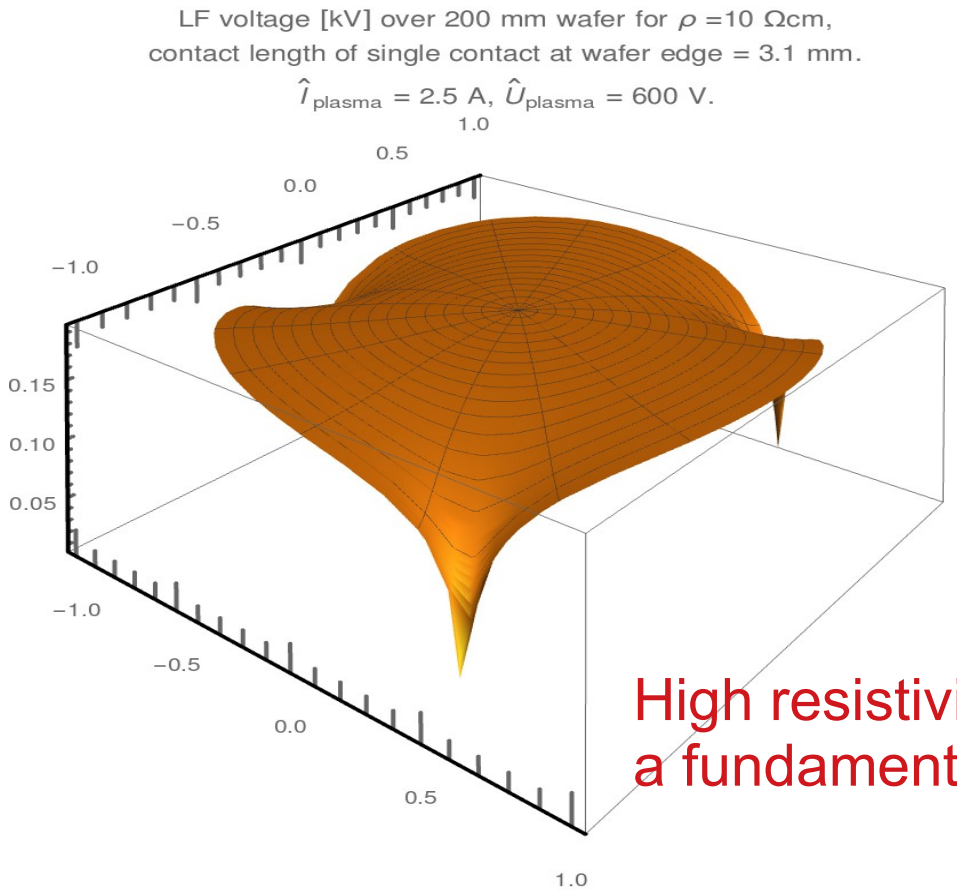
  The only relevant recipe parameters.

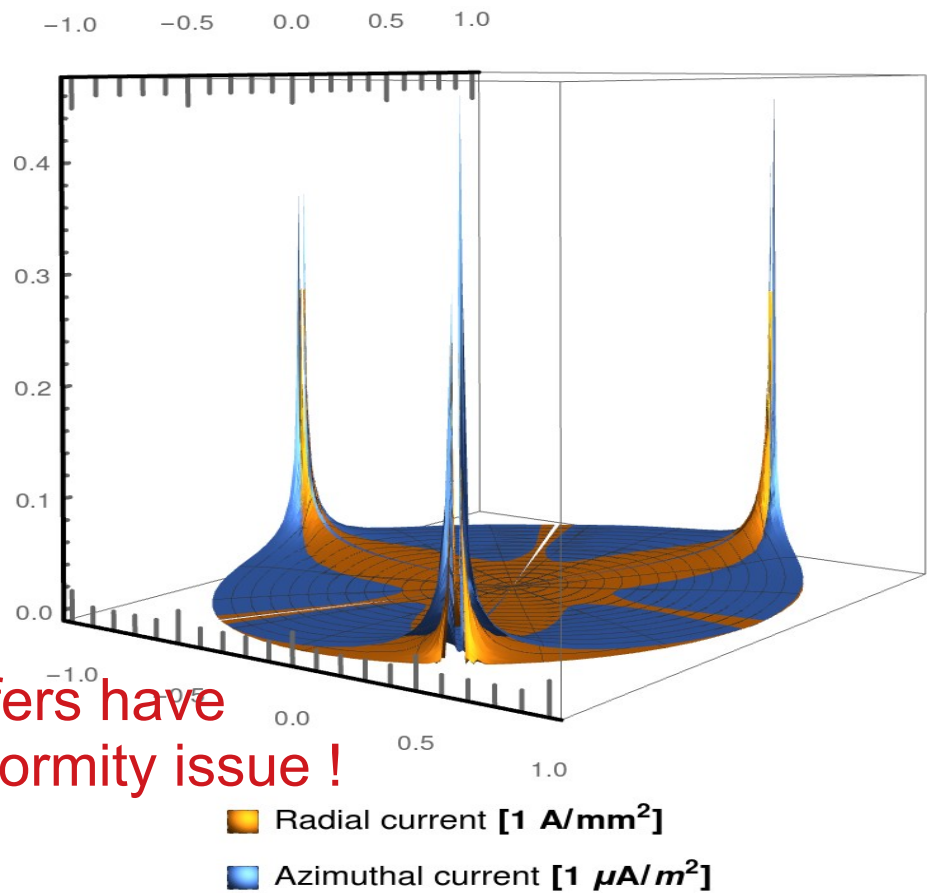
Voltage and current – 1 Ωcm & 3 mm contact





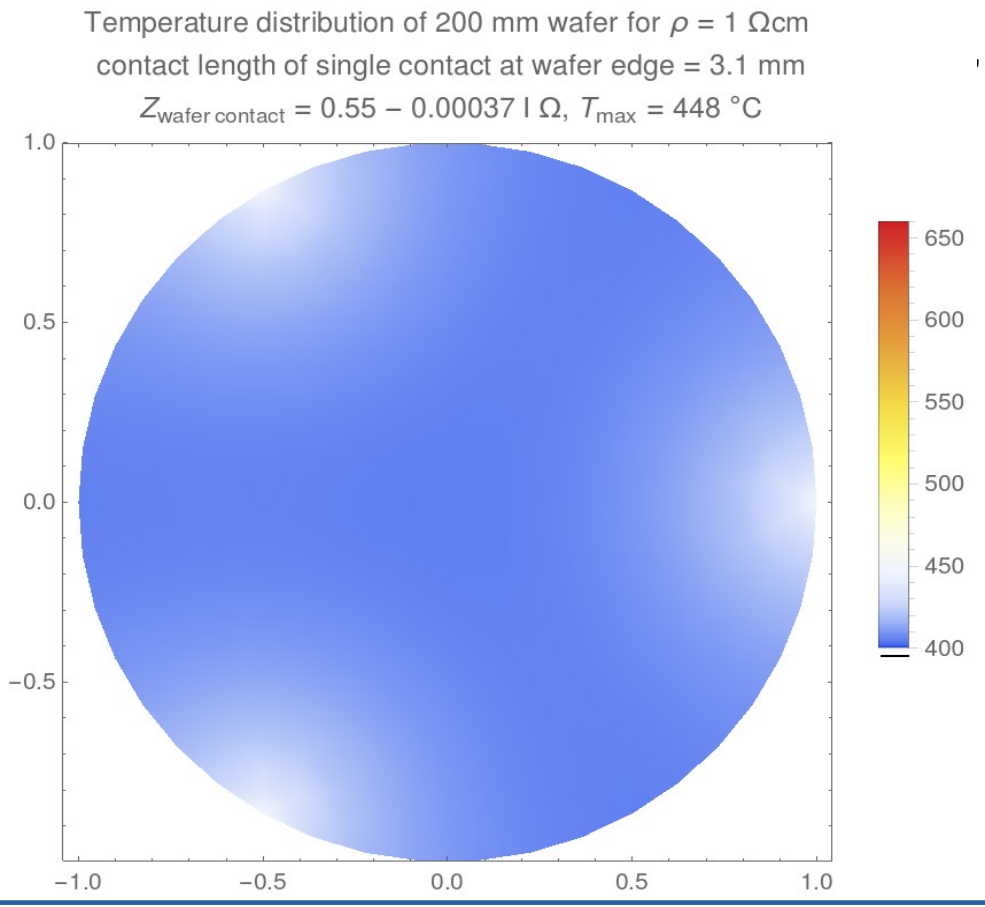
Voltage and current – 10 Ωcm & 3 mm contact



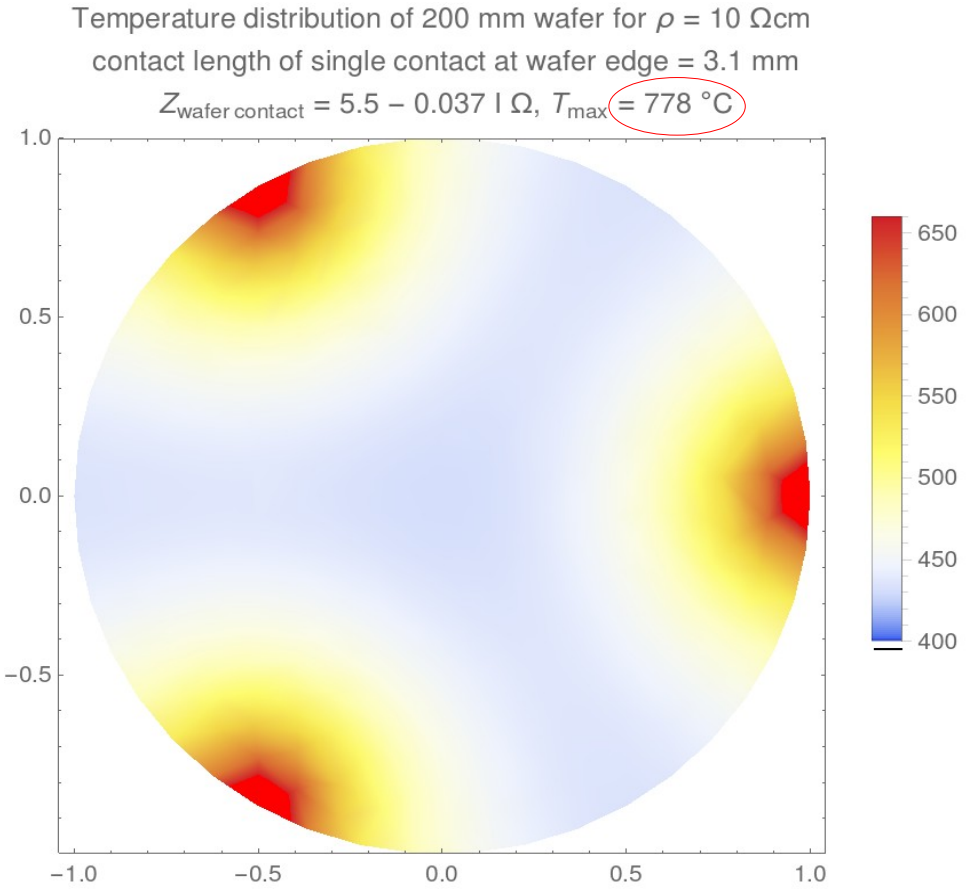


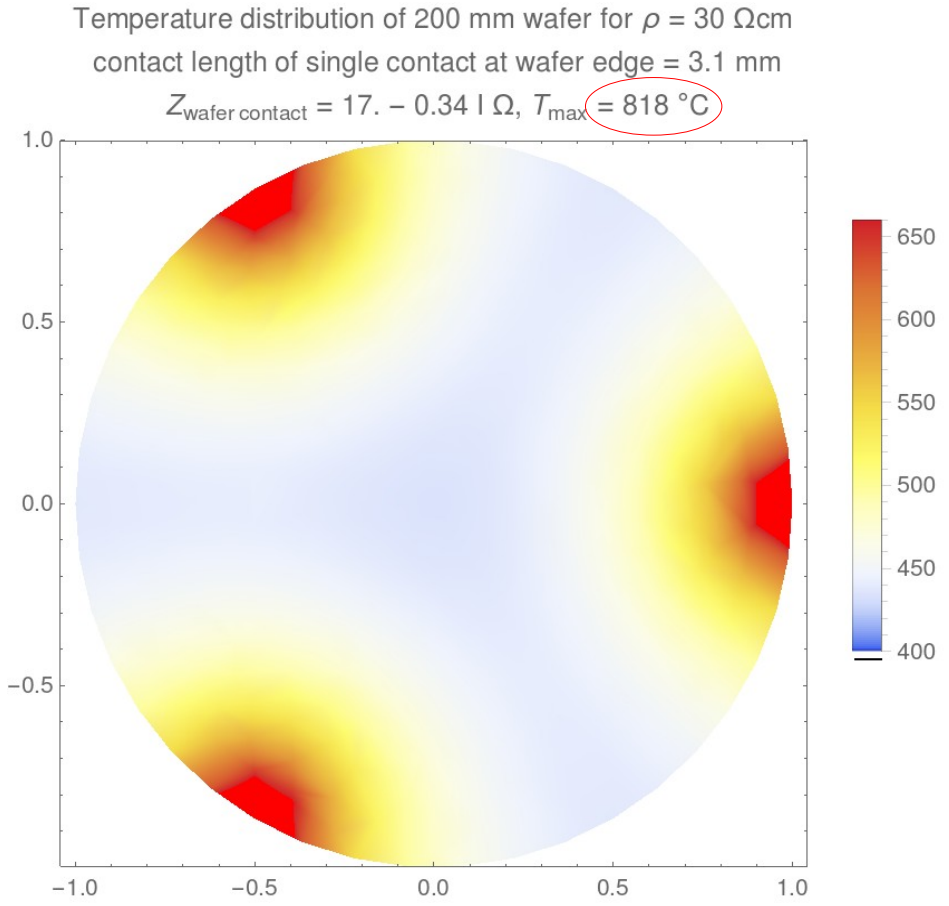
High resistivity wafers have a fundamental uniformity issue !

Temperature distribution – 1 Ωcm & 3 mm contact

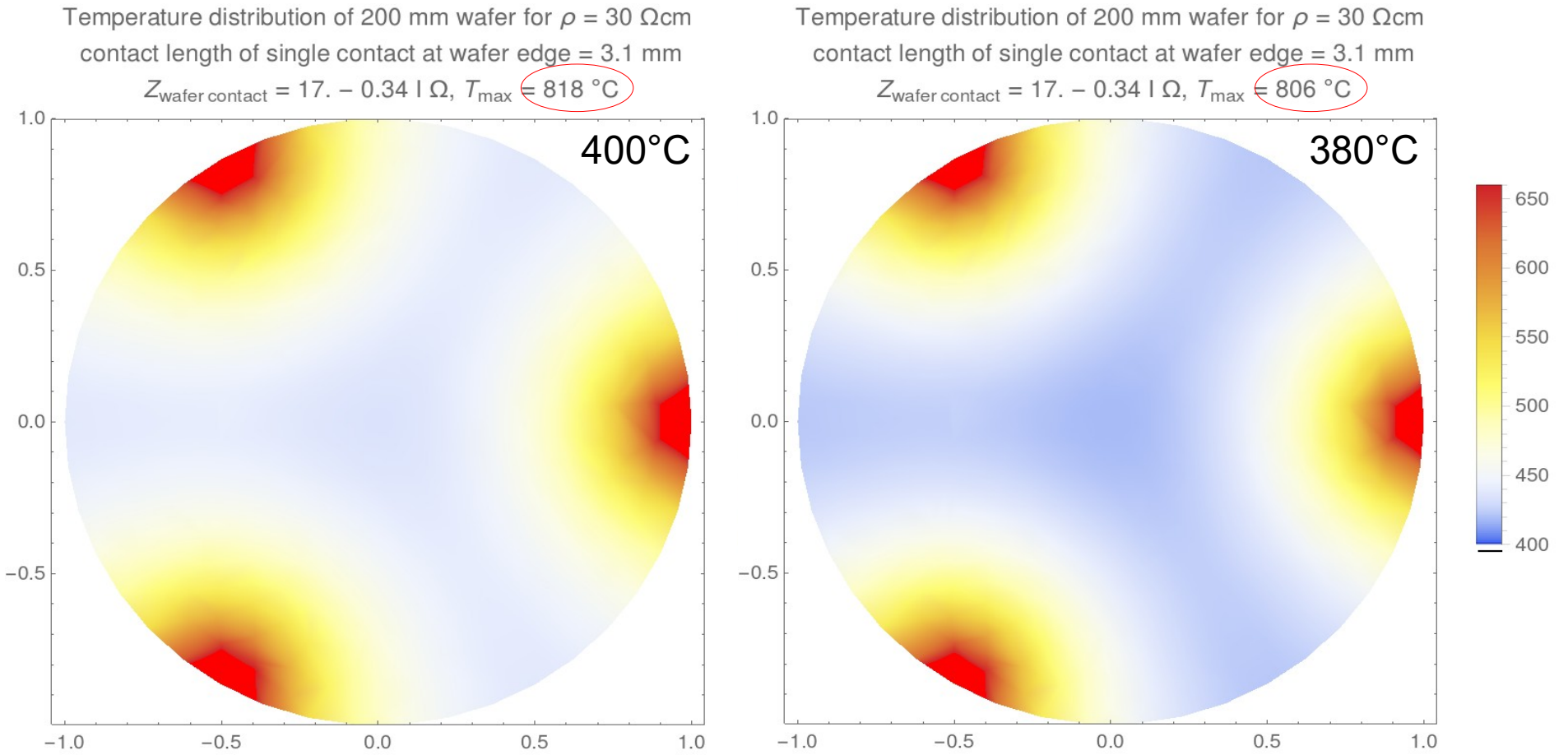


Temperature distribution – 10 | 30 Ωcm & 3 mm contact

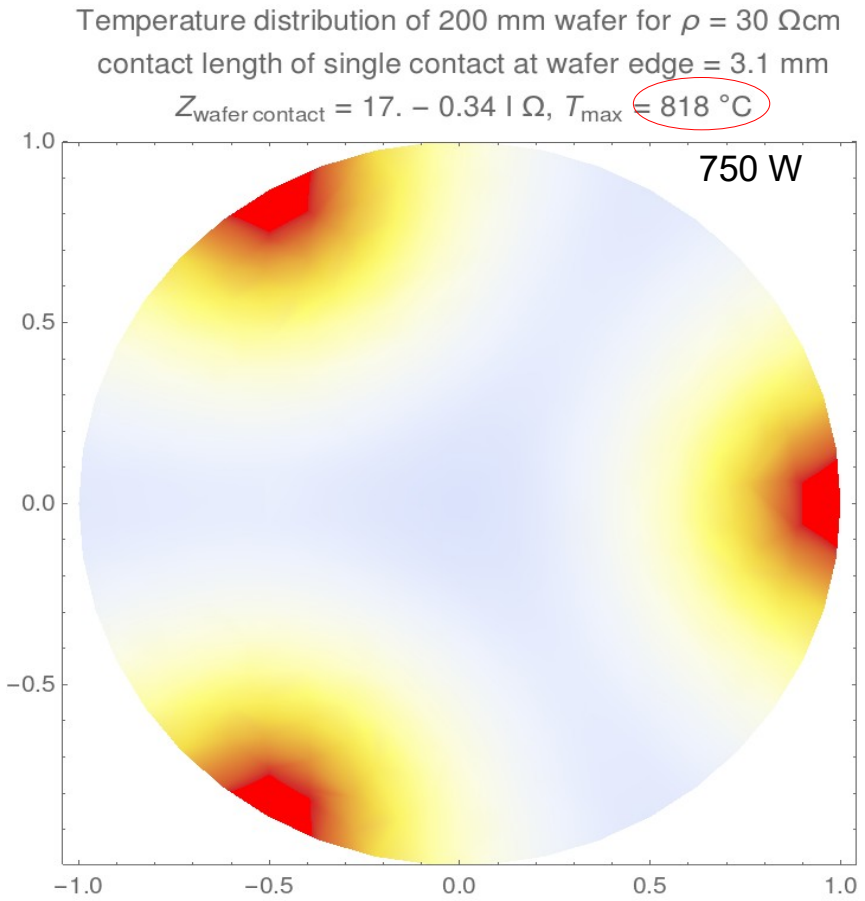


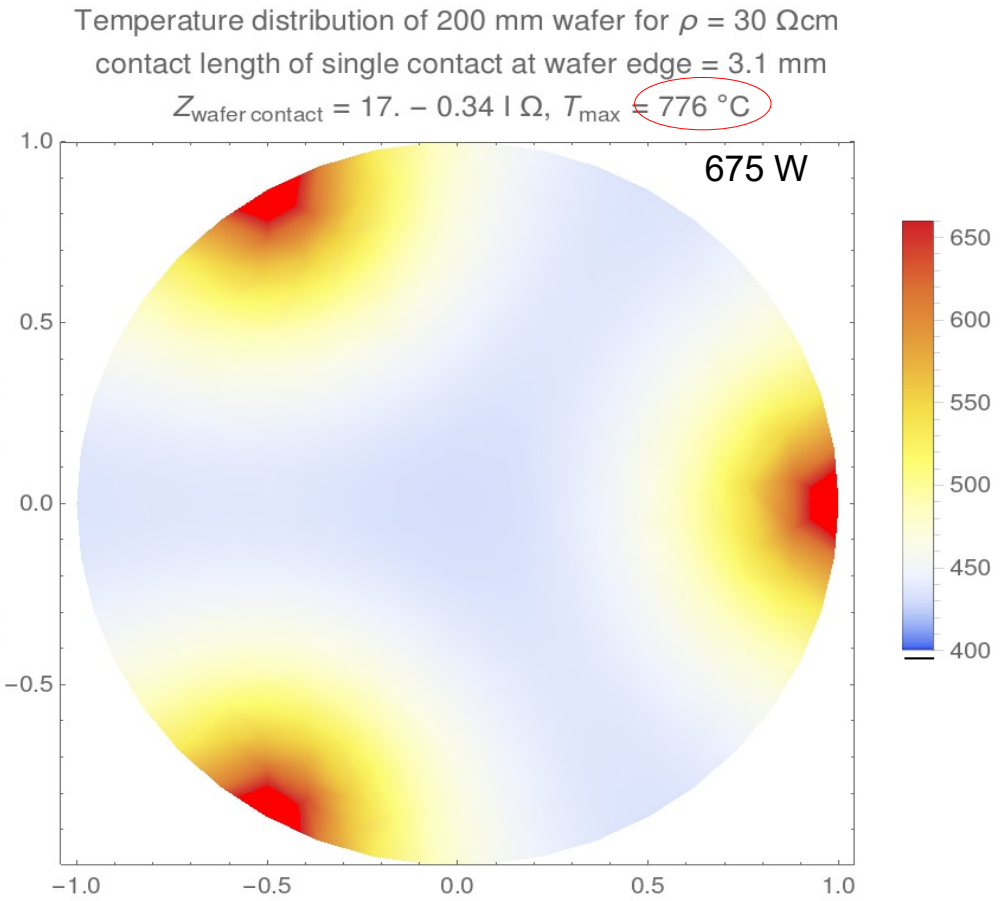


Decrease of chuck temperature by 20°C

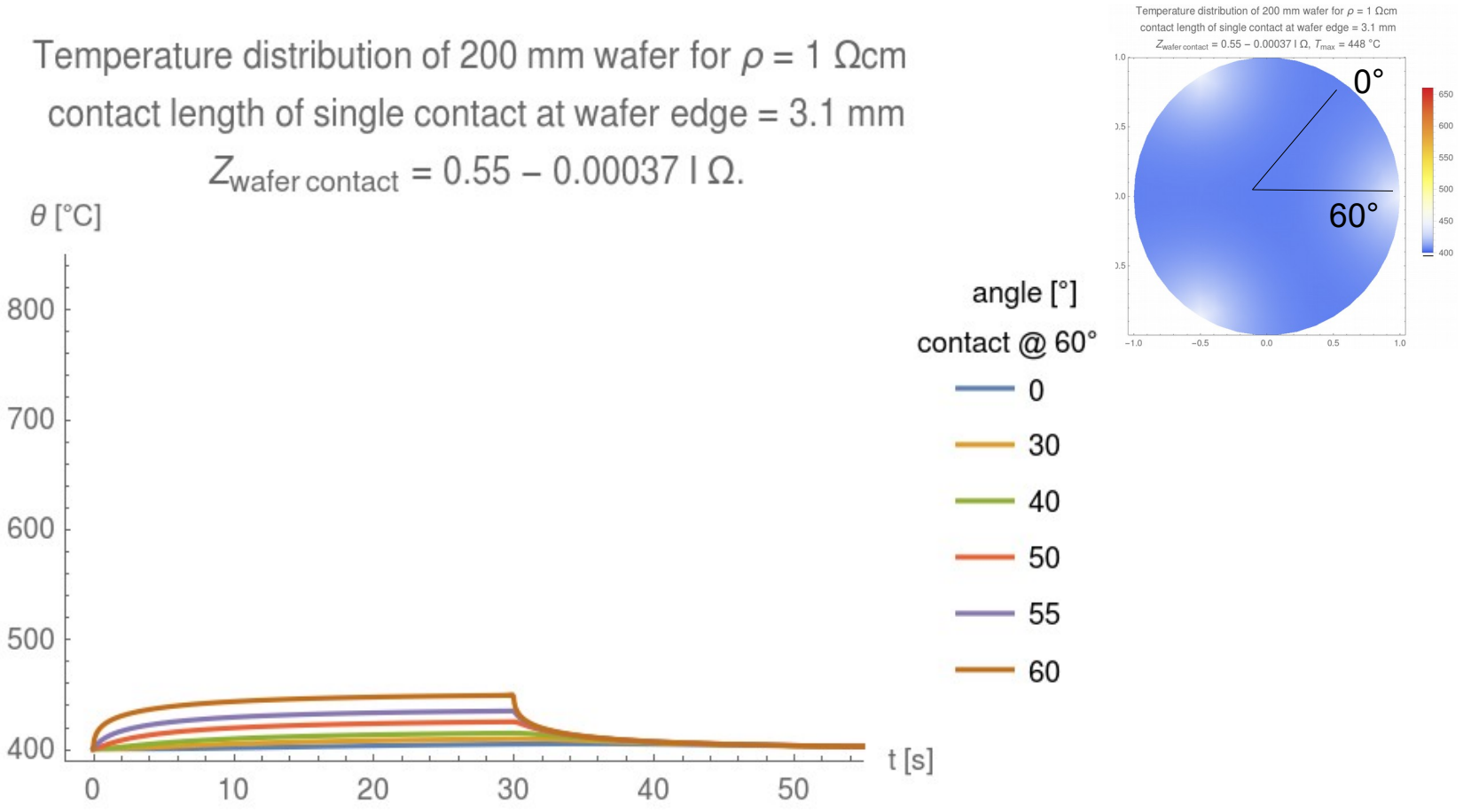


Decrease of LF power by 10 % – not really sufficient → Chemistry !

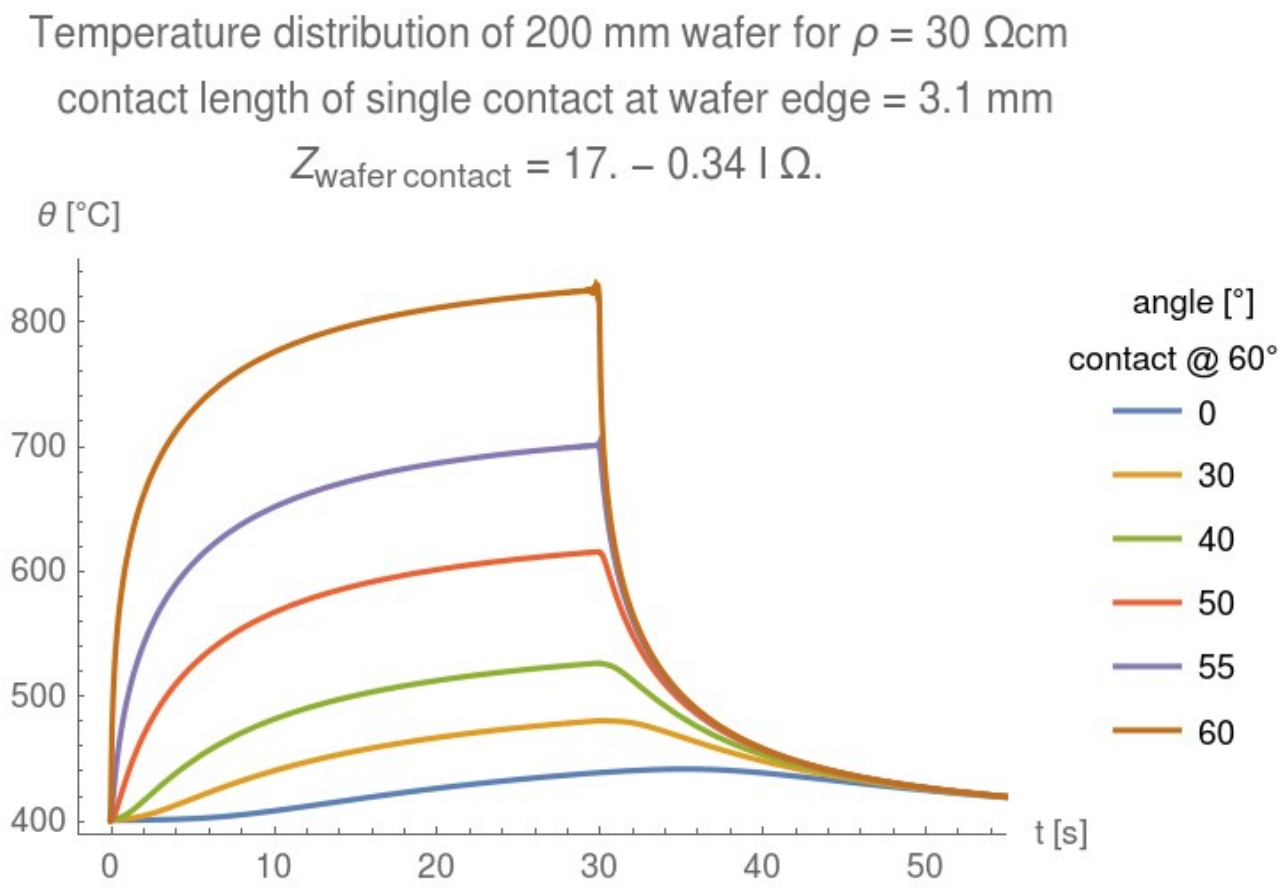




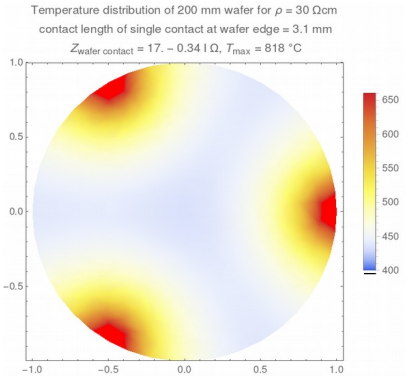
Temperature over time – low resistivity



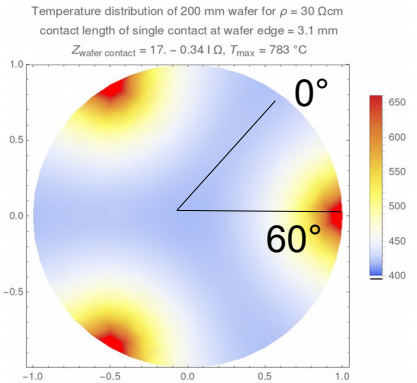
Temperature over time – high resistivity

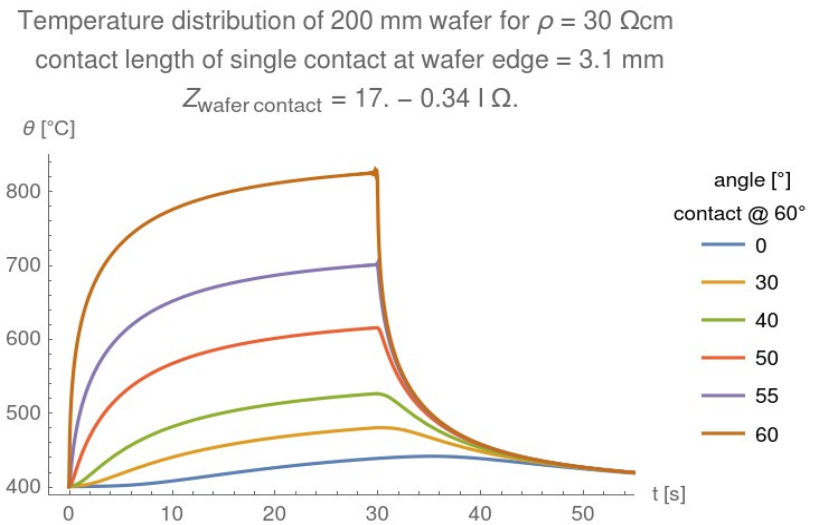


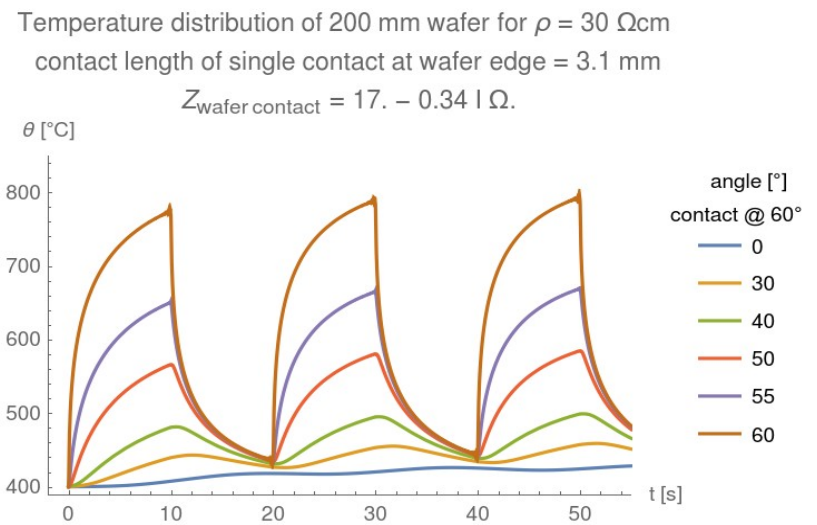
Temperature over time with break – higher resistivity



Mean temperature and duration of high temperature decreased by break in plasma steps.
Additional break recommended !







Conclusions

- Methodology of digital twin
  - RF equipment model
  - Electrical plasma model
  - Thermal model
  - Excellent process understanding

- Results
  - Breakdown (wafer arcing) and local Via heating are very unlikely.
    → Electrical Si heating depending mainly on contact and resistivity
  - There is a heavy dependence on wafer resistivity
  - Usual parameter variations does not work

- Solution
  - Insertion of process break, wafer cools down quickly – mainly by radiation, set only LF power to 0, all other parameters should be kept constant.

- Already verified via splits runs, no via up extrusions an longer.