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Arcing prevention by dry clean optimization using plasma parameter monitoring

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Die Verantwortung für den Inhalt dieser Veröffentlichung liegt beim Autor.

Overview

- Shallow Trench Isolation (STI) etch process - Overview
- The problem
- Experimental Sequence (Overview)
- Basic experiments with CF_4/O_2 Cleans
  - etchrate vs. O_2 - concentration
  - electron collision rate vs. O_2 - concentration
  - clean influence on Conditioning - wafers
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- Experiments on product wafers
- Summary
- Outlook

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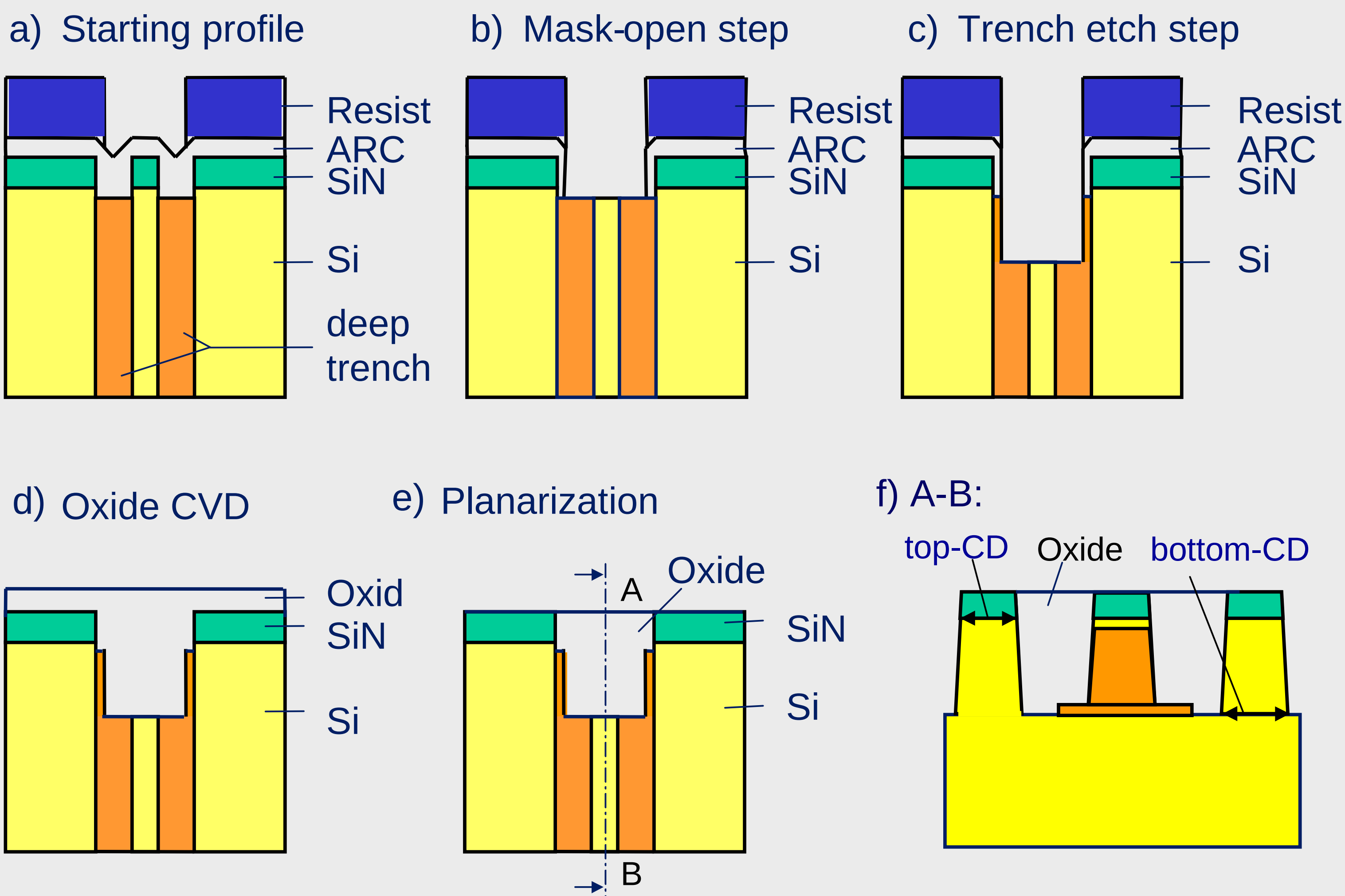
STI etch process - Overview



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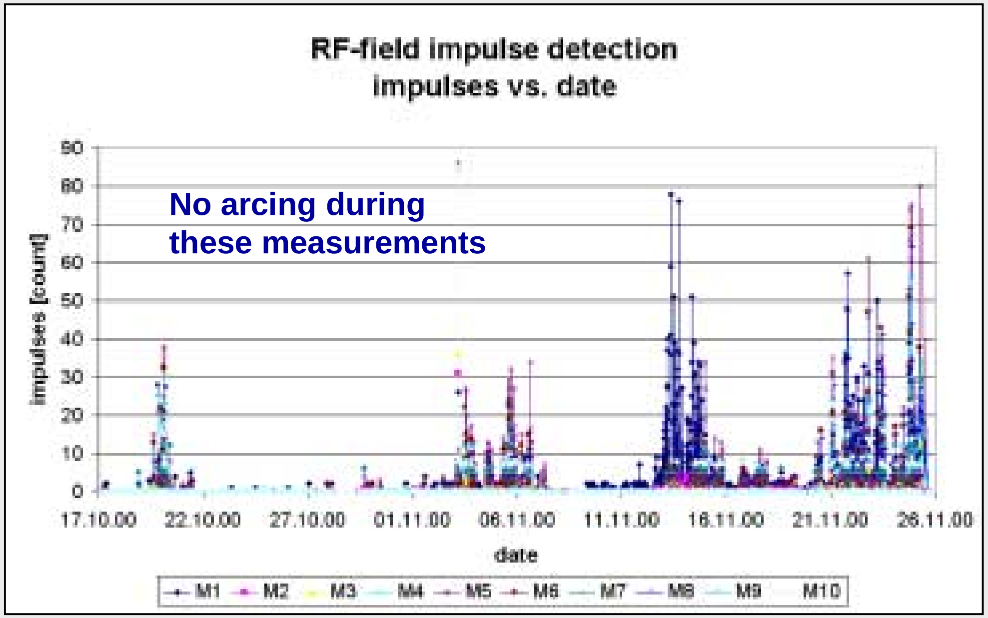
The problem (motivation)

- New DRAM product ➔ new recipe for STI etch necessary
- New recipe generates more chamber wall polymers
  - increased arcing danger
  - more extensive chamber cleaning
- New dry clean for wall polymer reduction used
  - reduces wall polymers, but
  - **C**ritcal **D**imension (CD) on product wafers effected
- ➔ New dry clean recipe needed with:
  - effective wall polymer reduction (simultaneously reduces arcing danger)
  - no CD degradation on product wafers

Joined application of impulse detection in the RF stray field and SEERS to fix the arcing problem



- Illustration of impulses observed in RF stray field outside the chamber over one wetclean cycle
- Very high sensitivity, many impulses, but no arcing observed

- Combination of two real time in-situ measurement techniques to solve arcing problem:
  - Impulse detection in the RF stray field outside the chamber will detect breakdowns of the electromagnetic field caused by micro arcing
  - Plasma parameters will help to optimize dry clean and detect heavy arcing

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Experimental sequence

- Determination of suitable O_2 and CF_4 concentration
- best dry clean recipe tested on resist wafers
- Shorter clean step - test on resist wafers
- Dry clean with conditioning step - test on product wafers
- Changed conditioning step recipe - test on product wafers
- Variation of clean- / conditioning time - test on resist wafers

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Basic experiment with CF_4/O_2 dry cleans (DC)

	O2 sccm	CF4 sccm	Gesamt sscm	O2 %	CF4 %
1	50	10	60	83,3	16,7
2	50	13	63	79,4	20,6
3	50	50	100	50,0	50,0
4	30	30	60	50,0	50,0
5	10	50	60	16,7	83,3

Experiment	Cond	DC 1	Cond	DC 3	Cond	DC 4	Cond	DC 5	Cond	DC 2
Etchrate meas.	DC 1	DC 3	DC 4	DC 5	DC 2					

- Test of dry clean recipies by measurement of resist etch rate on test wafers
- 5 dry clean (DC) - recipes with varying O_2/CF_4- ratios to figure out a working recipe
- First part of experiment:
  run conditioning wafers to recondition chamber before each clean

Dependence of etch rate on O_2 - concentration (resist test wafers)

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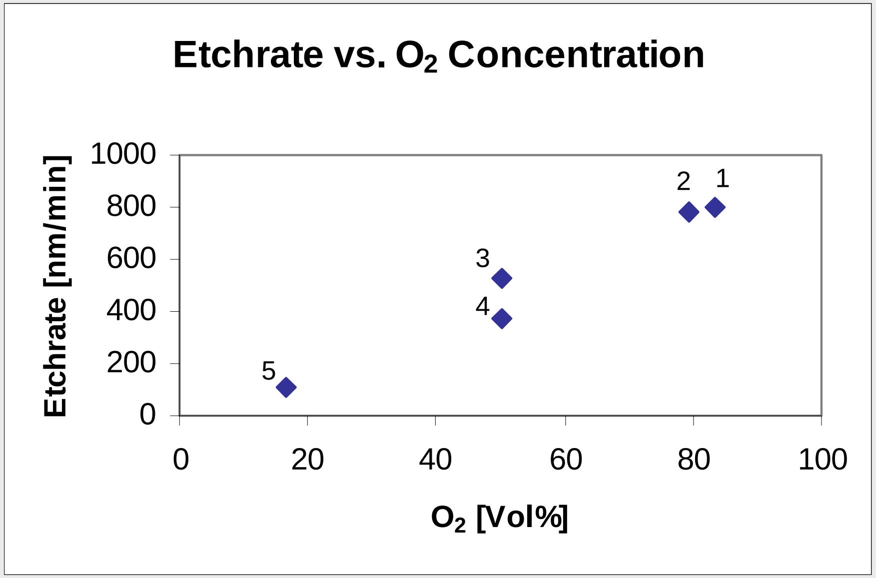

- Highest etch rates in case of O_2 - concentration being much higher than CF_4-concentration (dry clean 1 and 2)
- Lowest etch rate in case CF_4 dominates (dry clean 5)
- Higher etch rate with higher total gas flow (dry clean 3 vs. dry clean 4)

Dependence of electron collision rate on O_2 – concentration: Bare Si-wafers vs. resist wafers

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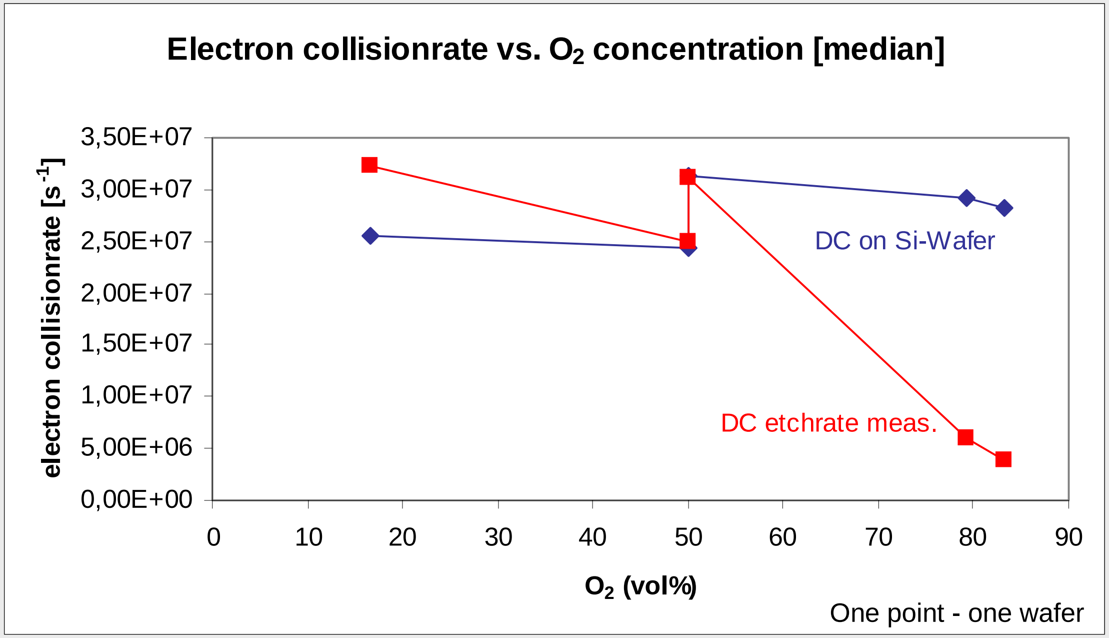

- The higher the O_2 -concentration, the lower the electron collision rate in dry clean - test at etch rate measurment (red curve)

- But: there are big differences in electron collision rate depending on type of wafer used
  - DC on Si- wafer doesn‘t have such a big influence on plasma as DC on resist wafers, because of less reaction products from wafer surface (blue curve)

Impact of dry clean on chamber conditioning as measured by monitoring electron collision rate

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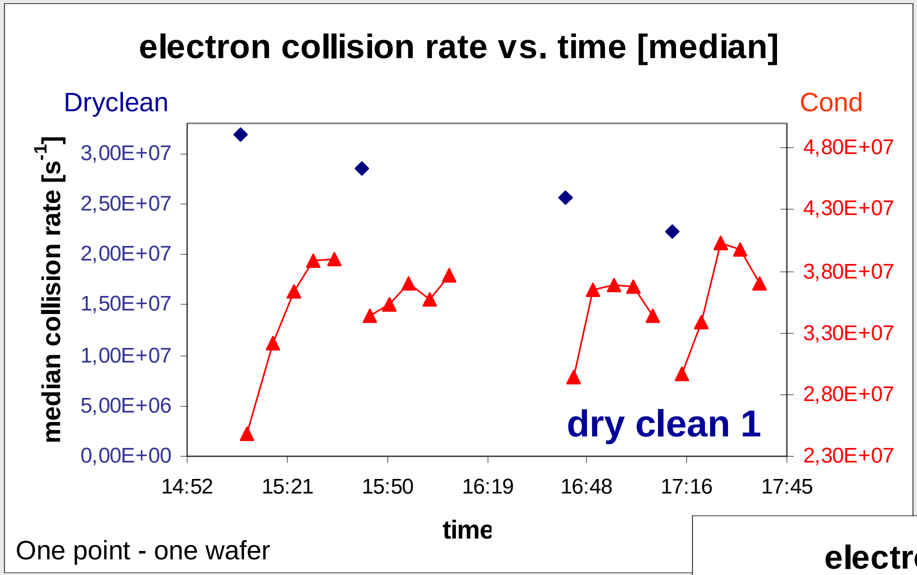
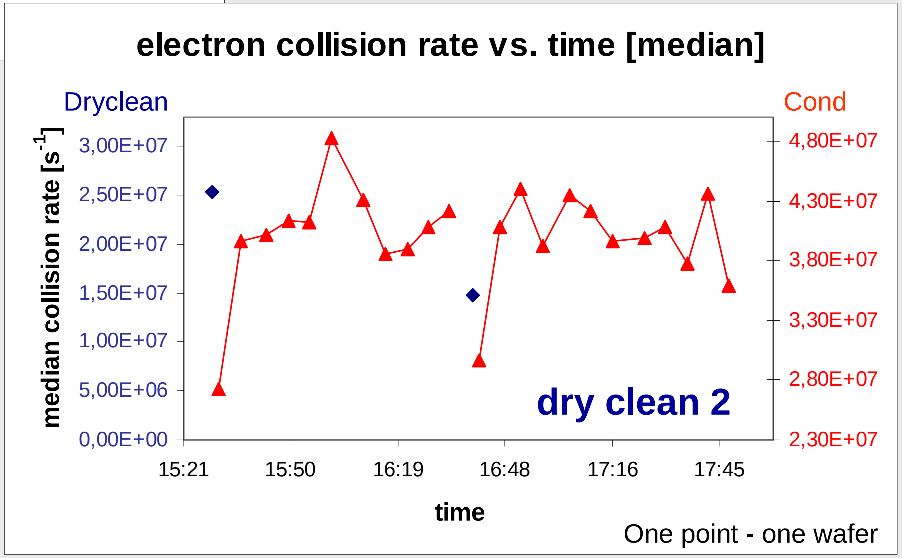


- ❑ Comparison of two different dry clean recipies
- ❑ Variation of process time: dry clean 1 > dry clean 2

- ❑ First wafer effect depends on clean time:
  dry clean 1: 2 ... 4 wafer
  dry clean 2: 1 wafer
- ❑ Clean process indicates long term chamber drift



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Basic experiments - summary

- General problem:
  - Etch rate is measured on resist test wafers on the cathode
  - It does not reflect etch rate of polymers on the chamber walls directly
- Result of basic experiments: With higher O_2 – concentration:
  - ➔ higher resist etch rate on test wafers
  - ➔ lower electron collision rate in plasma
- Dry clean with high O_2 - concentration was chosen for further experiments
- First wafer effect strongly depends on process time of dry clean. But even short dry clean shows significant impact on first wafer after clean.
- Conclusions:
  - Application of a conditioning step after clean to reduce first wafer effect
  - Ratio between clean step and conditioning step has to be optimized

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Experiments on product wafers

- Experiments on product wafers were done with dry clean recipe chosen from basic experiments (high O_2 concentration)
- Questions:
  - Does dry clean influence the process on product wafers in the same way as on resist test wafers ?
  - What´s the impact of the CF_4/O_2 dry clean on critical dimensions (CD) at STI etch ?
- ➔ Variation of
  - Conditioning recipe
  - Clean step time
  - Conditioning step time
- Targets:
  - Minimize of first wafer effects and
  - Maximize of polymer reduction at chamber wall

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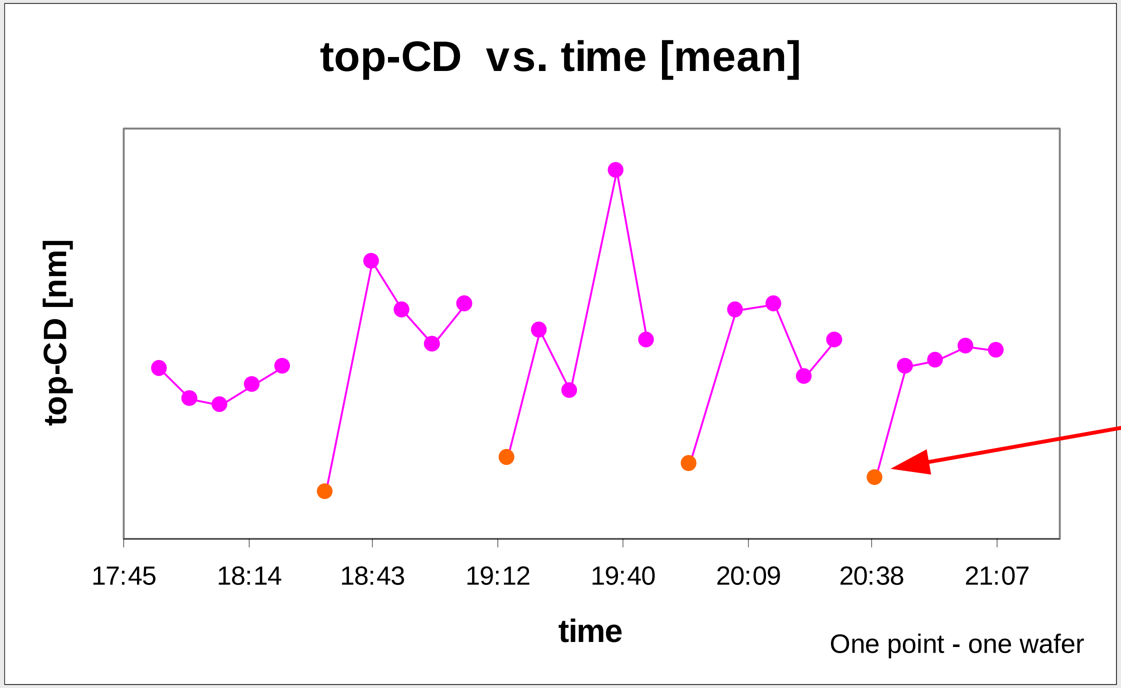
Impact of dry clean with conditioning step on product wafers: Critical Dimensions



- First wafer effect is indicated by critical dimensions, measured on product wafers
- ➔ Chosen dry clean process with conditioning step has still significant impact on critical dimensions at STI etch

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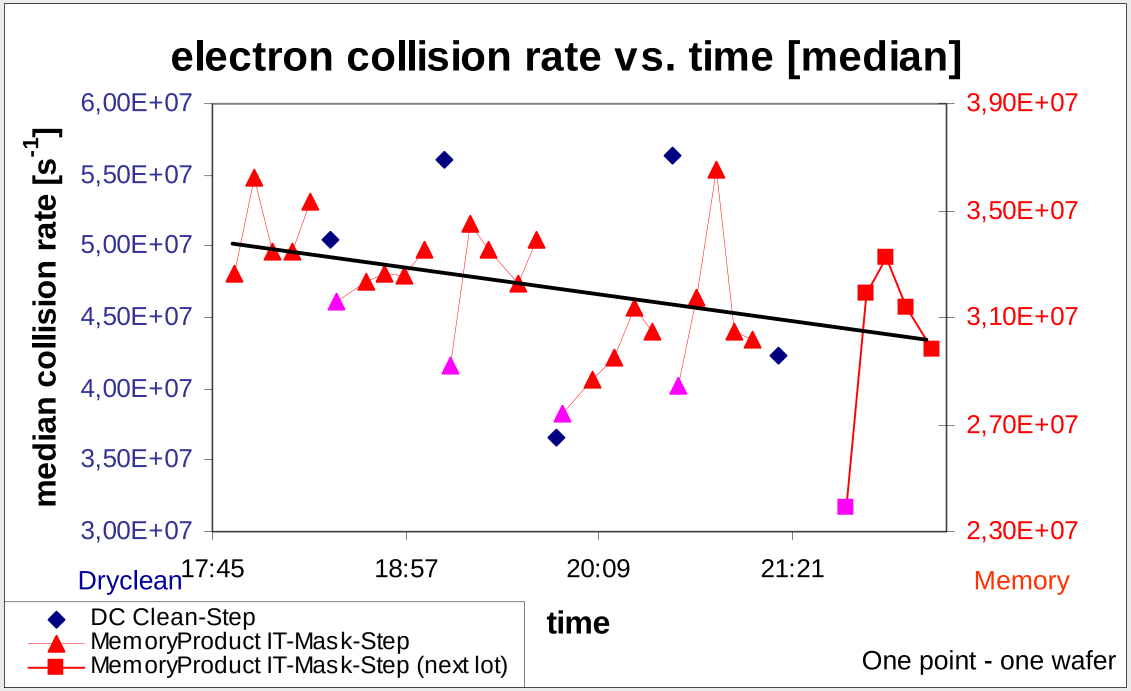
Impact of dry clean with conditioning step on chamber conditions – electron collision rate on product wafers



- First wafer effect, caused by dry clean, is indicated by electron collision rate
- Additionally electron collision rate indicates drift of chamber conditions (mean down trend)

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Correlation top - CD vs. electron collision rate

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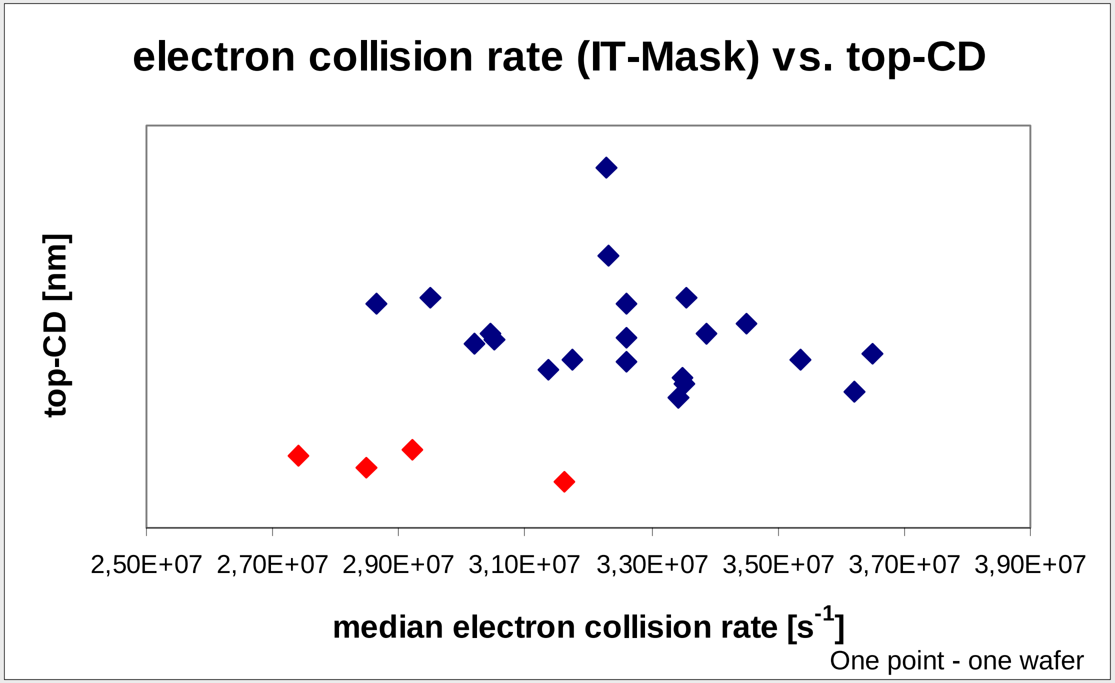

- Red points represent first product wafers after dry clean
- Electron collision rate vs. top- CD does not correlate, although red points are seperated from others è because of low top- CD

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Impact of dry clean conditioning step without CF_4 / O_2 on Critical Dimension

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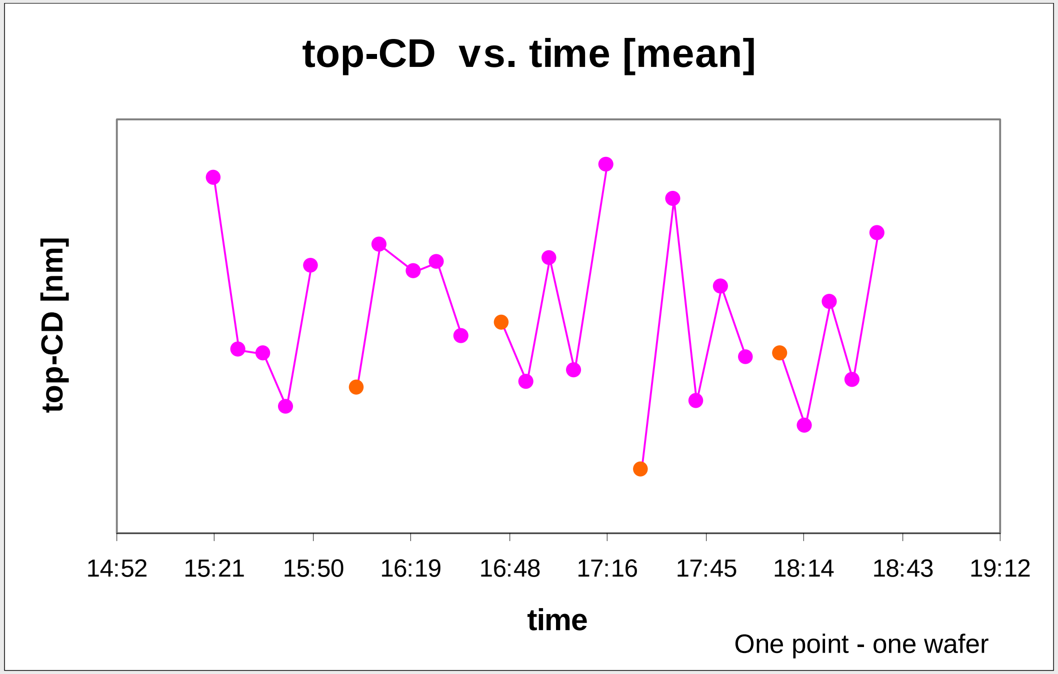
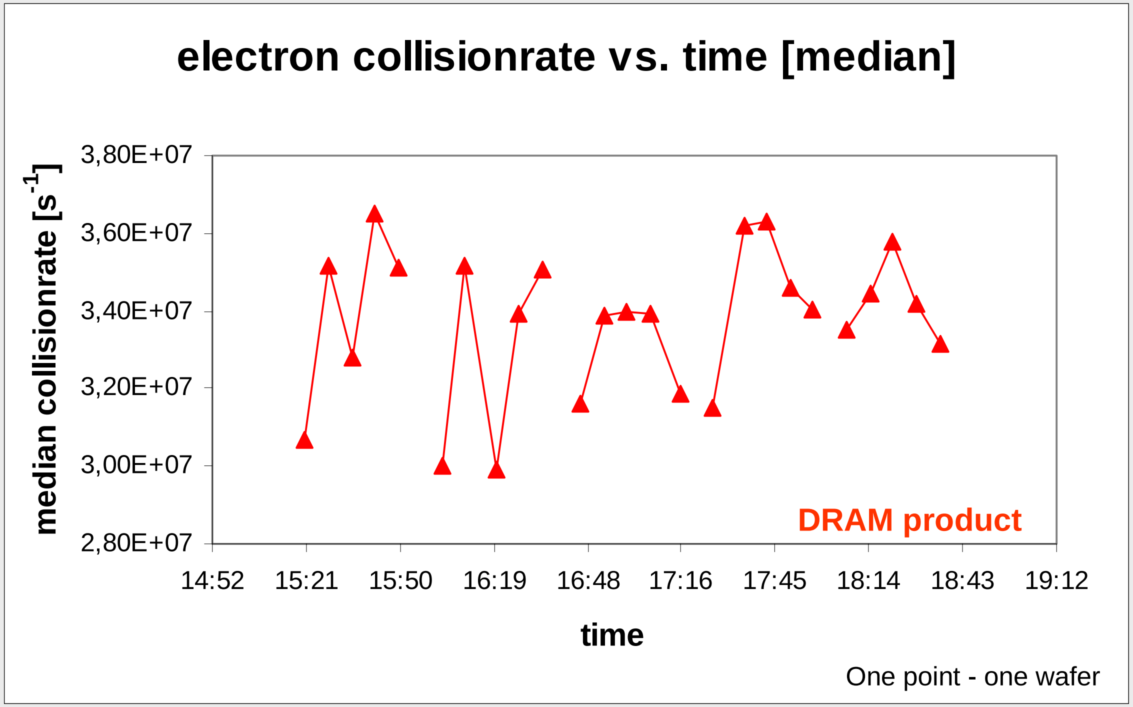


- Dry clean with CF_4 / O_2 in clean step, but no CF_4 / O_2 in conditioning step now !

- Now dry clean doesn‘t seem to have a big influence on critical dimensions
- But: is dry clean still as effective? Polymers are generated in the conditioning step and without CF_4 / O_2 even more ➔ possibly the clean effect is spoiled by the following conditioning step ?)

Electron collision rate at conditioning step without CF_4 / O_2



- No significant first wafer effect after each dry clean

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Variation of clean time and conditioning time

- Notation:
  - Clean**L** - long clean (used in last experiments)
  - Clean**S** - short clean
  - Cond**L** - long Conditioning
  - Cond**S** - short Conditioning (used in last experiments)
- Experiment in 3 runs on resist test wafers:
  - Clean**L**/Cond**S**
  - Clean**L**/Cond**L**
  - Clean**S**/Cond**S**

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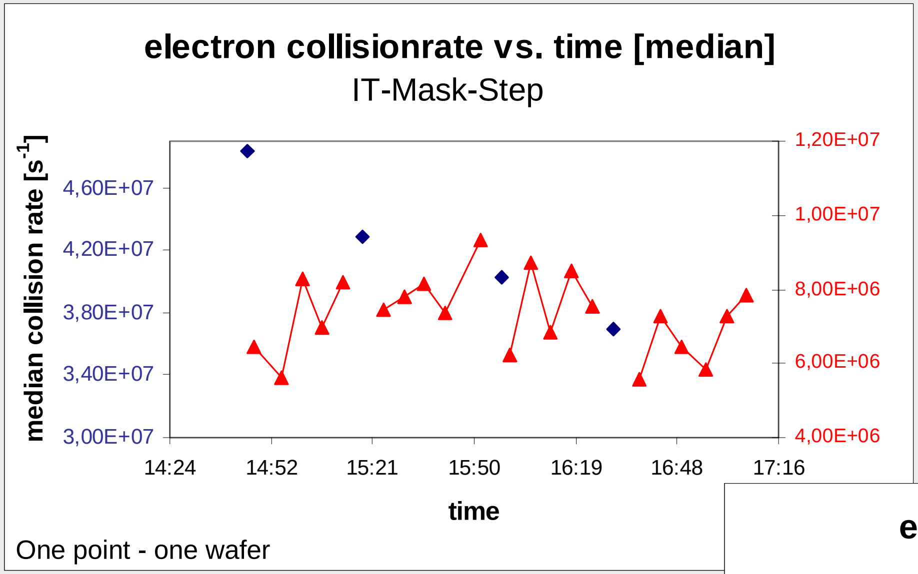
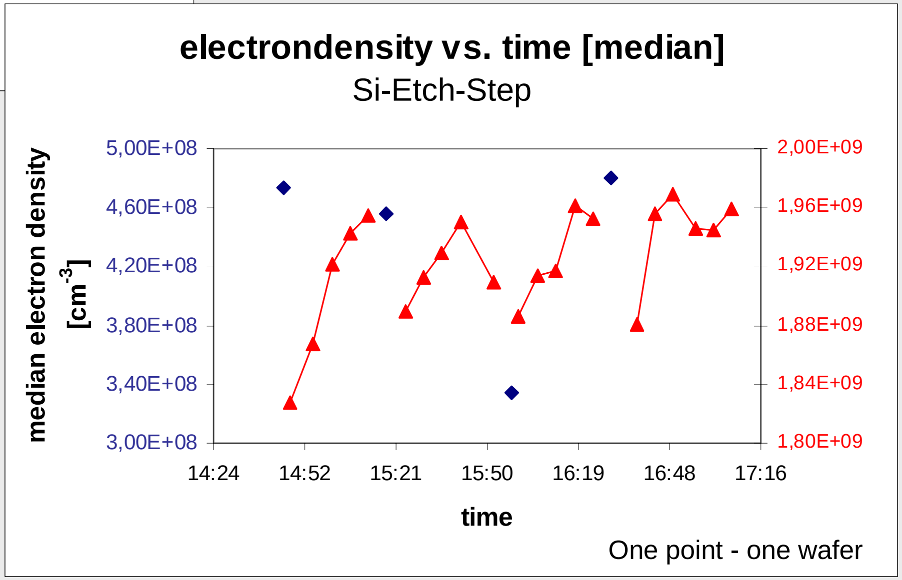
CleanL / CondS: comparison of plasma parameters



- There is ***no*** significant trend in collision rate of resist wafers after each dry clean ...
  - ...as it was seen previously with CF_4 / O_2 in conditioning step or even without conditioning step

- But now there ***is*** a trend in electron density of resist wafers after each dry clean
  - plasma parameter response has changed with change in dry clean recipe !



Comparison of electron density for CleanL / CondS and CleanL / CondL

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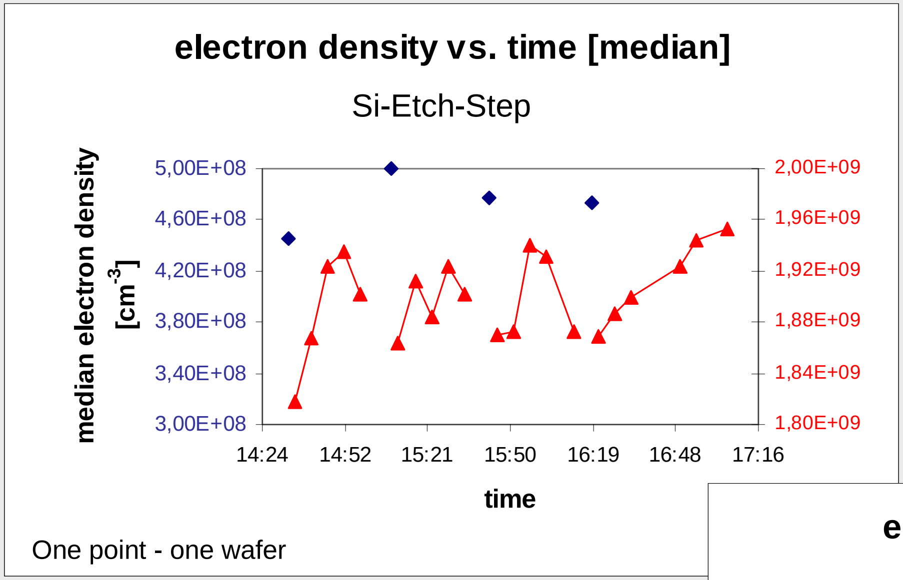
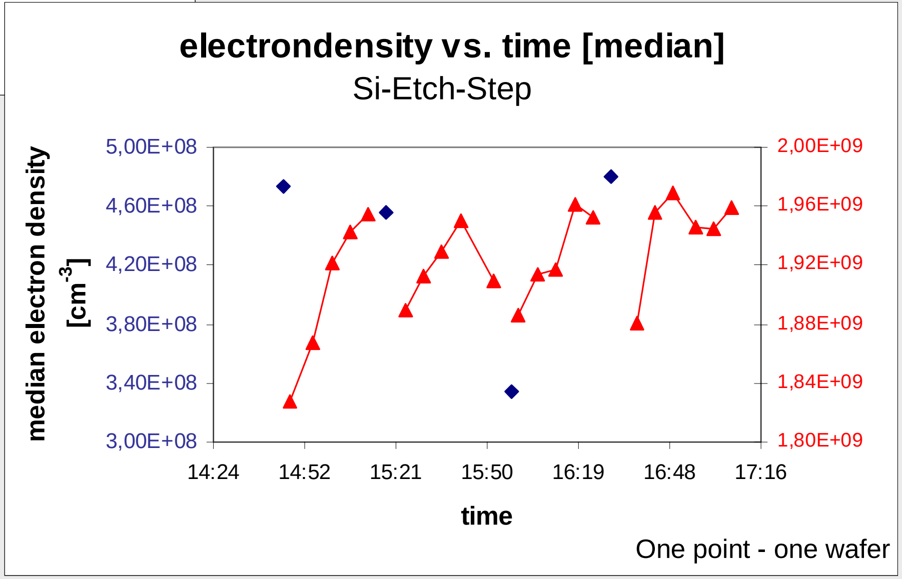


CleanL/CondL

CleanL/CondS



- Longer conditioning time doesn‘t seem to cause changes in trend of electron density of following resist wafers

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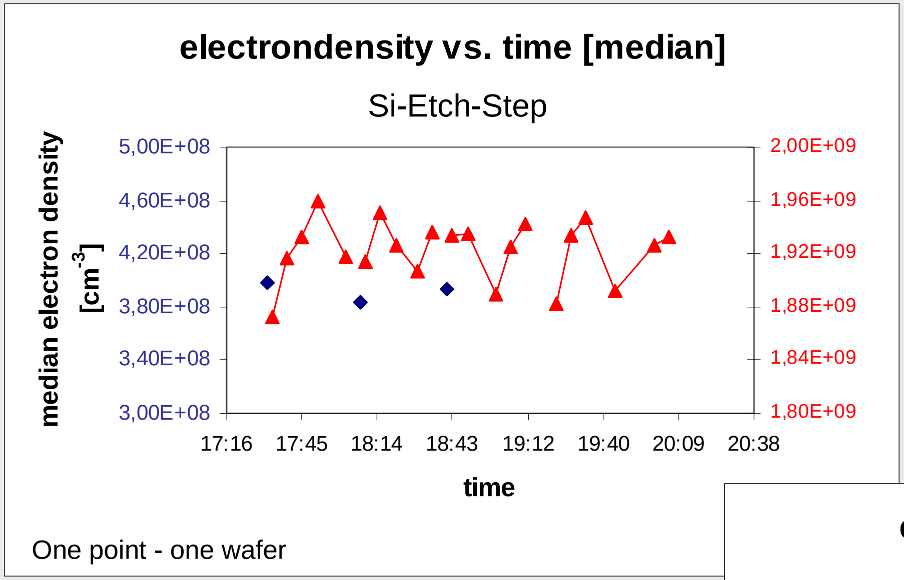
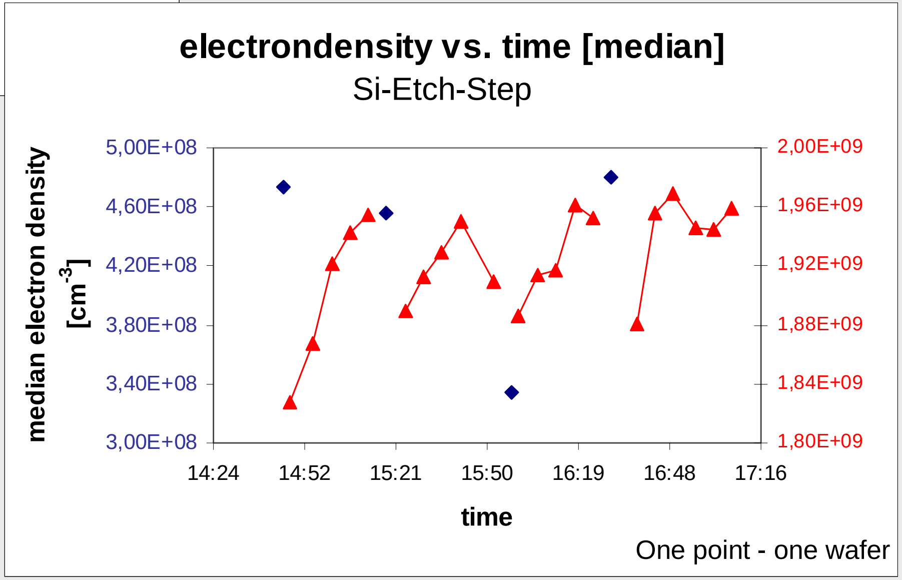
Comparison of electron density for CleanL / CondS and CleanS / CondS



- Shorter clean time reduces first wafer effect on following resist test wafers
- But shorter clean means less polymer reduction at chamber walls !

Clean**S** **/** Cond**S**

Clean**L** **/** Cond**S**



Summary

- Electron collision rate and electron density have been used to optimize a new clean recipe at Shallow Trench Isolation etch in AMAT MxP chamber.
- Both plasma parameters show **in real time**
  - Dry clean impact on chamber conditions and first wafer effect on product wafers
  - **And** superimposed long term drift effects of chamber conditions
- The general problem is dry clean optimization by etch rate measurement on resist test wafers. However, wall polymers are etched as well!
- Because plasma parameters do indicate chamber condition drifts, they can be used to monitor clean efficiency with respect to wall polymers.
- Therefore plasma parameter measurements can significantly help to improve efficiency & reduce costs of dry clean process development.

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Outlook

- Dry clean optimisation from economic point of view (i.e. low cleaning incidence)
- Investigation of new dry clean efficiency, i.e. by determining polymer thickness before each wetclean
- Observation of inline parameters for products over long time
- Do plasma parameters at new dry clean behave in a different way, than they did at the old one (long time over one wet clean cycle) ?