Application of plasma parameters to characterize product interactions between memory and logic products at Gate Contact (GC) Stack etch in LAM TCP

Thomas Dittkrist
TU Dresden
Institut für Halbleiter- und Mikrosystemtechnik

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Thomas Dittkrist
TU Dresden
Institut für Halbleiter- und Mikrosystemtechnik

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Introduction

- Fundamentals of Field Effect Transistors
- Gate Contact Stack Etch (GC Etch)
- Problems with product mix
- Results of measurements in high volume production
- Conclusion
- Outlook

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TU Dresden
Institut für
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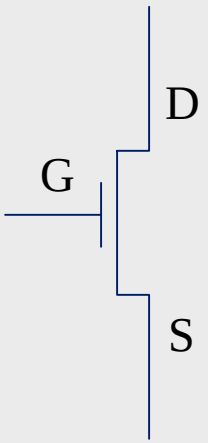
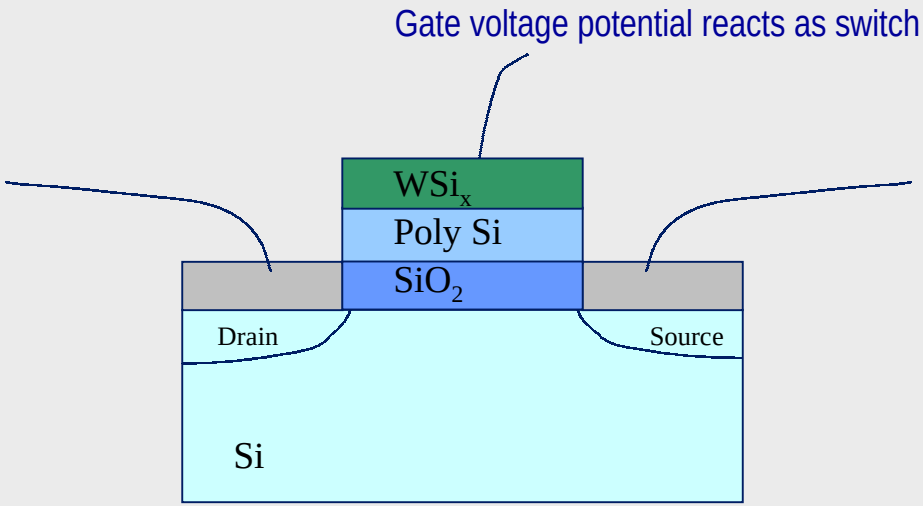
Fundamentels of Field Effect Transistor (FET)

- gate: part of FET to switch on and off transistor
- smallest dimension in transistor struction
- GC Stack etch important process step



symbol of FET device



Shematic cross view of FET

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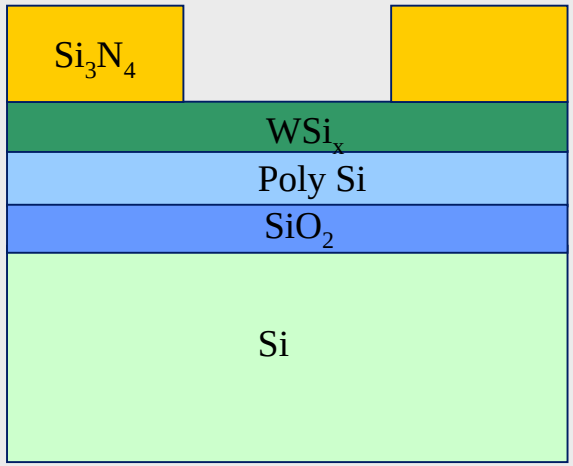
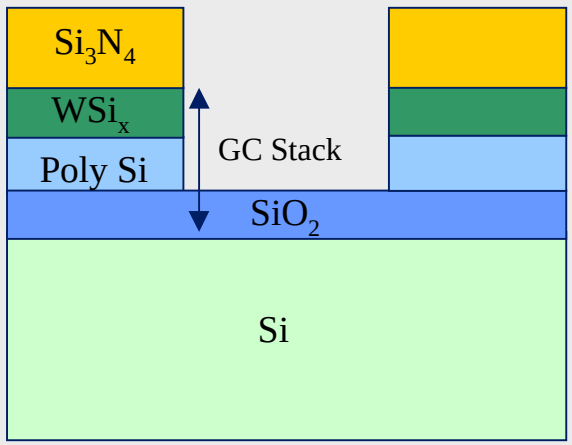
Gate Contact (GC) Stack Etch – a challenge of semiconductor processing



before etching



after etching

GC Stack etch process

- step 1 – plasma stabilization
- step 2 - WSi_x etch (endpoint stoped)
- step 3 - Poly-Si main etch (time stoped)
- step 4 - Poly-Si over etch I (endpoint stoped)
- step 5 - Poly-Si over etch II (time stoped)

Requirements of GC Stack etch process

- edges clean of Poly-Si
- no tungsten contamination
- no etch of SiO_2 layer
- high aspect ratio - steep sidewalls

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Problems with product mix

- different products (memory and logic) processed in same chamber
- important electrical parameters of logic products show serious drift depending on
  - Process mix at the chamber
  - Rf hours
- different products have various impact on chamber condition because of
  - Different recipes (plasma chemistry, rf power, etch time)
  - Different surface chemistry (open area, mask composition)

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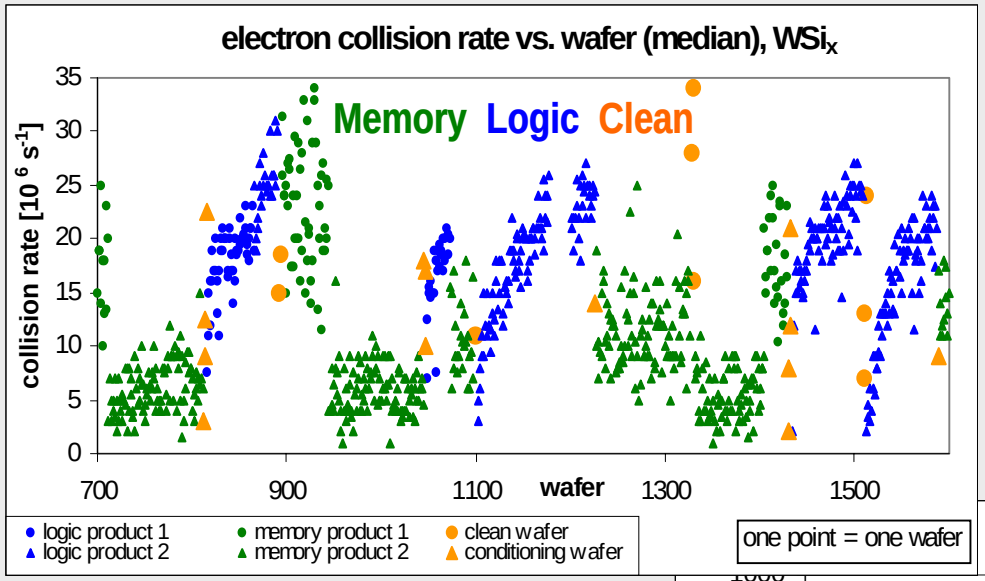
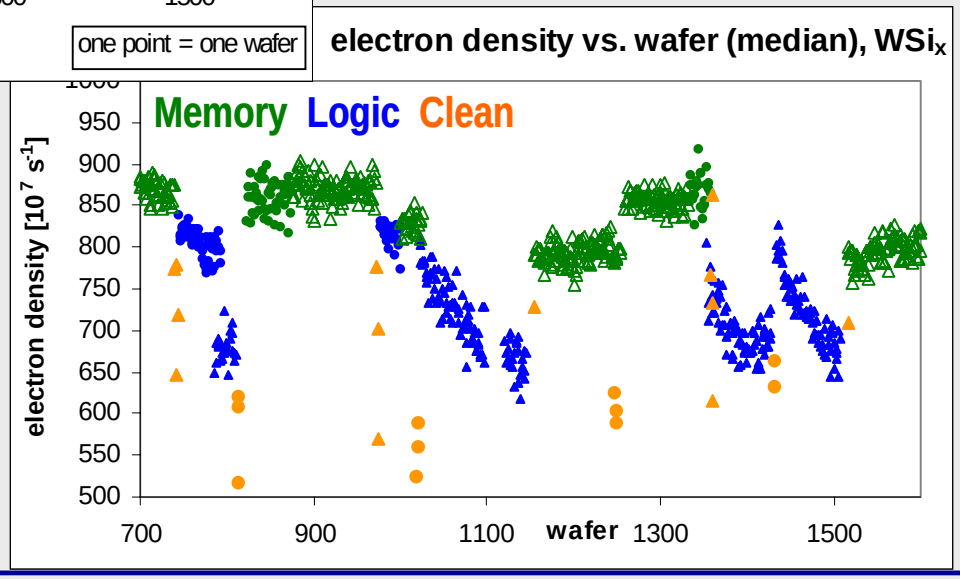
Comparison of collision rate and electron density



- collision rate goes up
- electron density goes down
- c.r. , e.d same tendency
- clean wafer same effect for collision rate and electron density

- Influence on collision rater bigger than on electron density
- for further considerations only collision rate used



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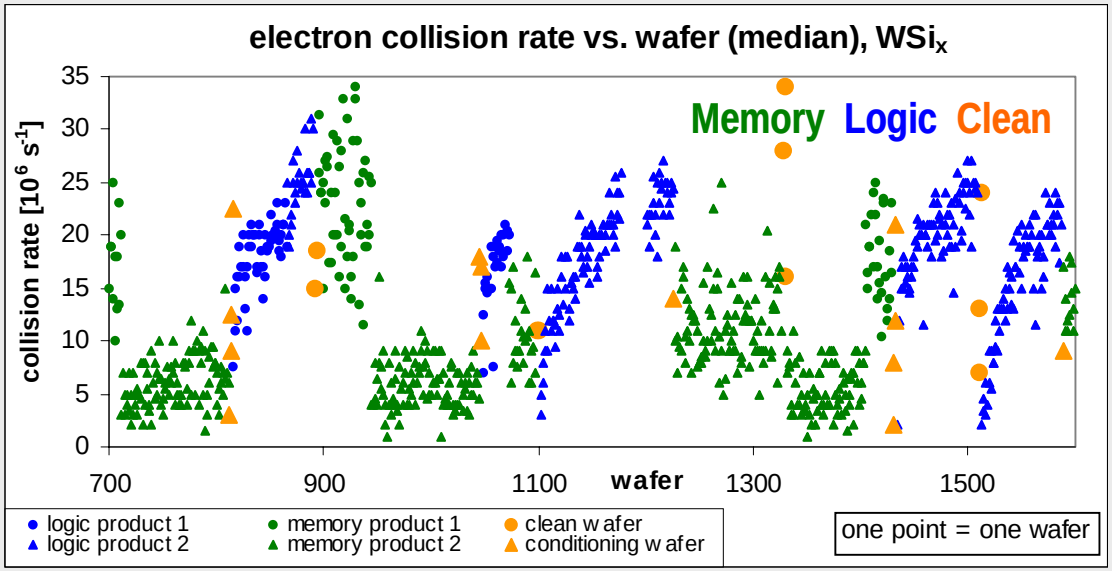
GC Stack, WSi_x etch
Electron collision rate versus wafer



- collision rate
  - increases over wafer number for logic products
  - logic - serious drift
  - memory - broad dispersion
- clean wafer before
  - logic product - collision rate goes down
  - memory product - no strong influence
- condition wafer
  - no big influence on collision rate

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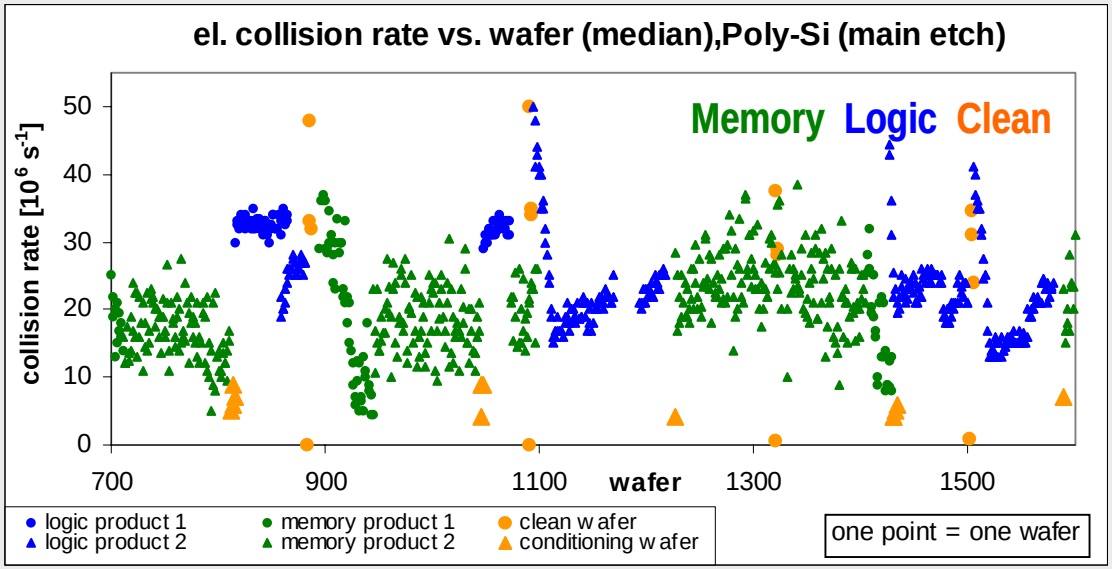
GC Stack, Poly-Si main etch
Electron collision rate versus wafer



- clean wafer before
  - logic product 2
    - collision rate goes up strongly
    - falls down during an initial phase
    - increases slowly after initial phase
  - logic product 1
    - no drift, no broad dispersion
  - memory product
    - not a strong influence

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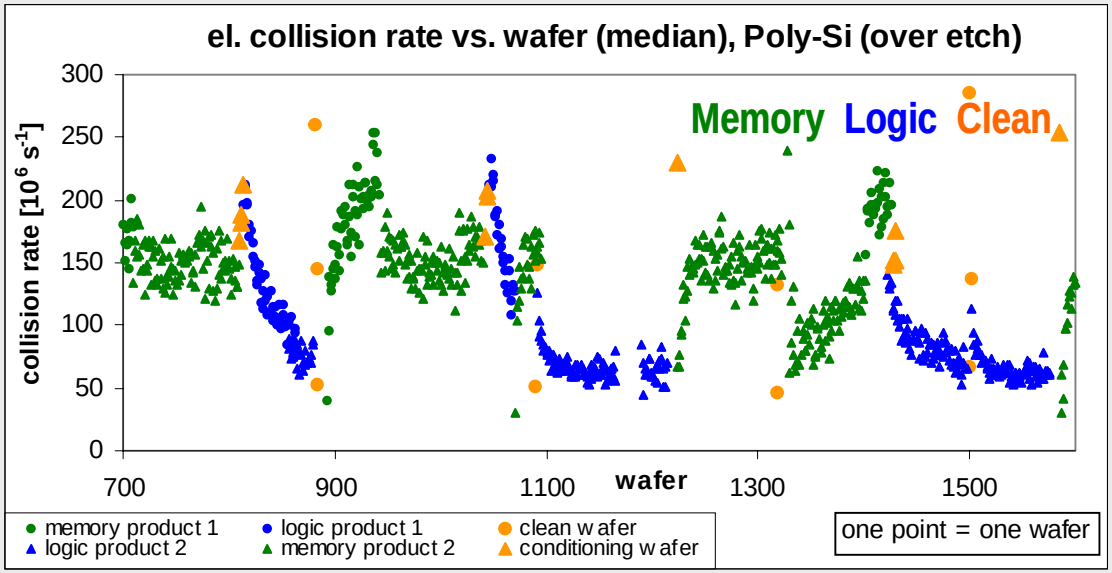
GC Stack: Poly-Si over etch
Electron collision rate versus wafer



- clean wafer before
  - logic product
    - collision rate goes up strongly
    - c.r. falls down to old level (saturation)
  - memory product
    - collision rate goes down
    - moves up again slowly

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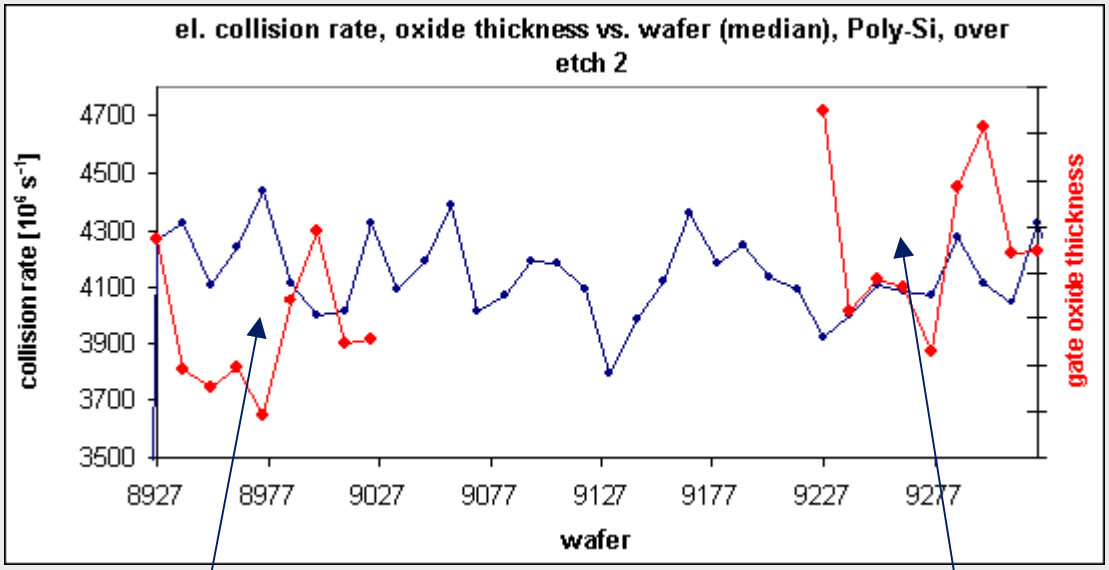
Correlation between gate oxide thickness and electron collision rate (Poly-Si, final over etch)



Correlation coefficient = -0,48

Correlation coefficient = -0,038

- same tendency of collision rate and SiO_2 thickness
- correlation not possible

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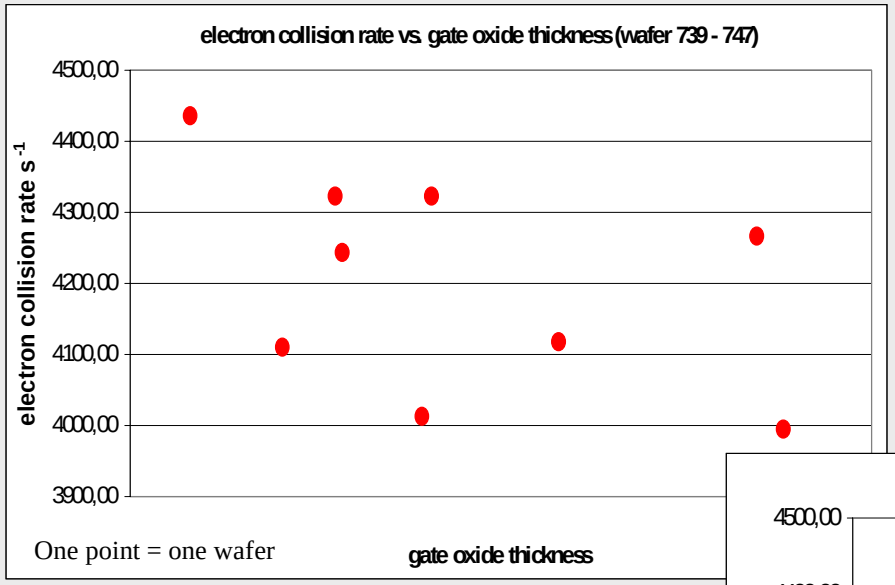
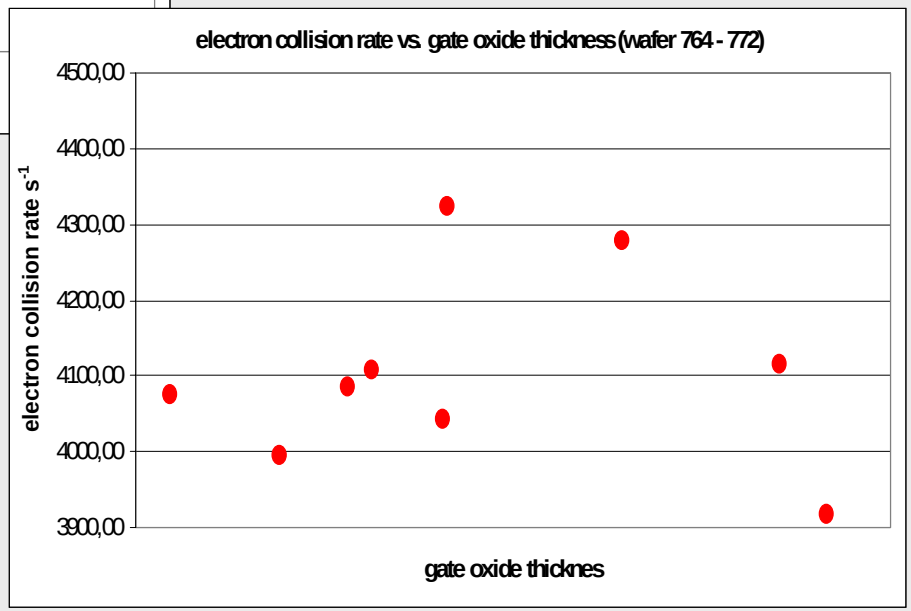
Electron collision rate versus oxide thickness



One point = one wafer

- not usable for process decisions
  - no clear tendency
  - broad dispersion



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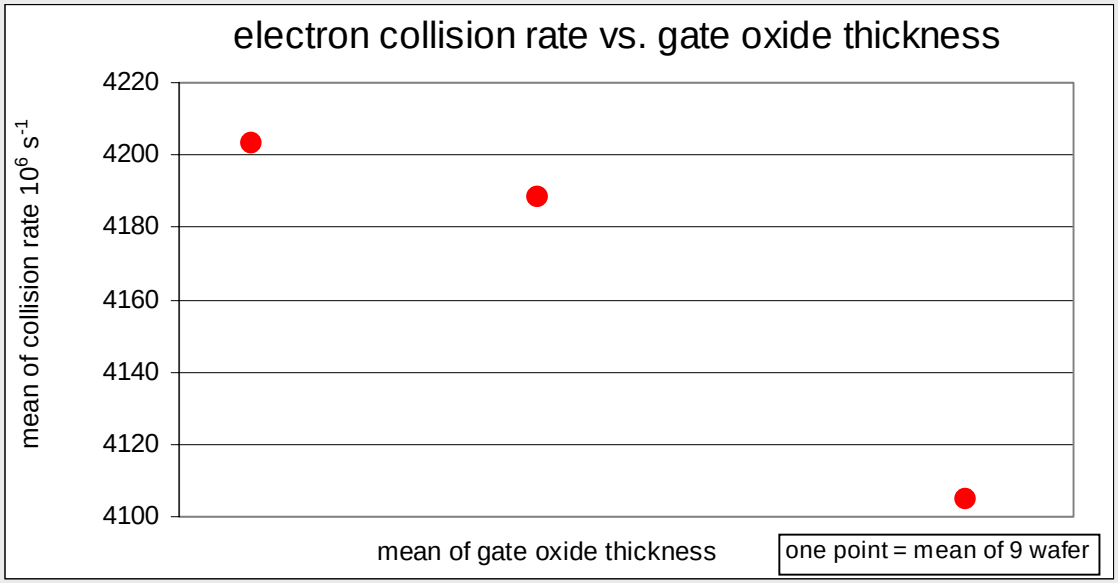
Mean of gate oxide thickness versus mean of electron collision rate (Poly-Si, final over etch)



- one point
  - mean of nine wafer processed after each other
- between points some hundret wafer processed without measuring
- after further research
  - collision rate maybe capable to detect serious problems with gate oxide thickness

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Conclusion

- collision rate capable
  - to detect product interactions
    - result - over etch responsible for product mix problem
  - to detect effect of clean wafer
    - good results for logic products at WSi_x etch
    - good effect after initial time at Poly-Si main etch
    - bad influence at Poly-Si over etch
  - to detect effect of condition wafer
    - no big influence on Plasma Paramaters
  - to detect tendency of gate oxide thickness

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Outlook

- comparison of plasma parameters with electrical data
- correlation between plasma parameters and etch results
- consideration of plasma chemistry
- interaction of chemical elements
- influence of plasma parameters on surface charging

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